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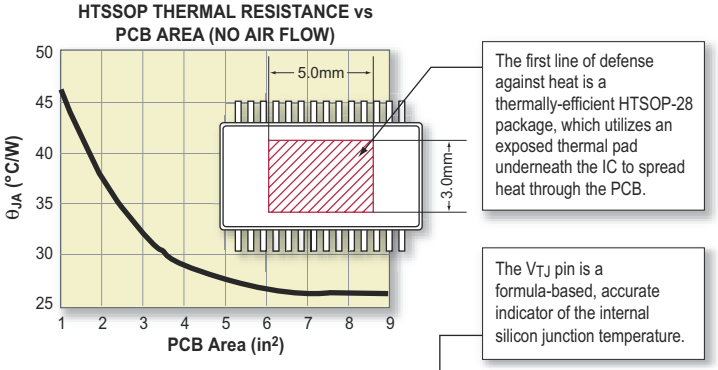
Maintaining IC temperatures doesn't have to be a riddle. Intersil's new high current Integrated FET Regulators have the industry's only true Thermal Protection with auto shut down at 135°C.

Intersil's EL7554 and EL7566 DC-DC buck regulators with internal CMOS power FETs operate from 3V-to-6V input voltage and are capable of up to 96% efficiency. But what's really cool about these devices is ground breaking features like built-in Thermal Protection and Voltage Margining for actual in-circuit performance validation.



The first line of defense against heat is a thermally-efficient HTSOP-28 package, which utilizes an exposed thermal pad underneath the IC to spread heat through the PCB.

The V_{TJ} pin is a formula-based, accurate indicator of the internal silicon junction temperature.

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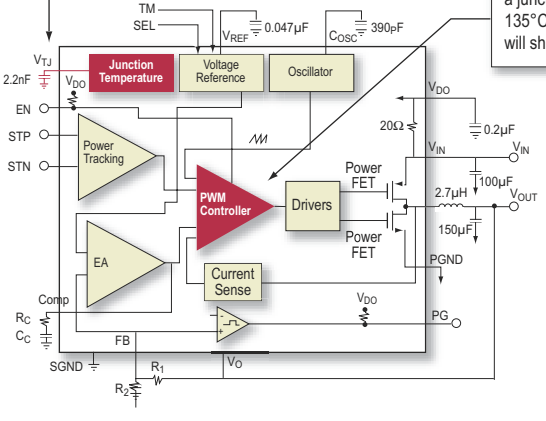

Key Features:

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- Built-in 5% voltage margining
- 3V-to-6V input voltage
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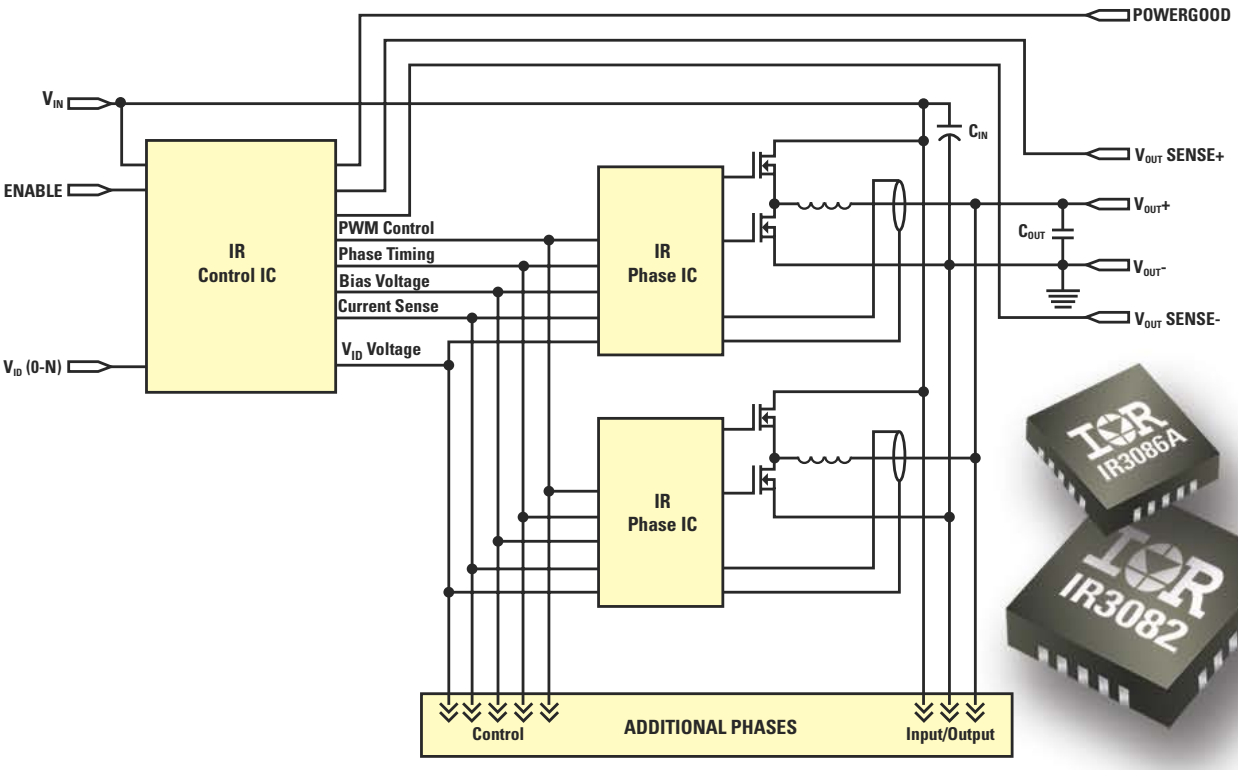

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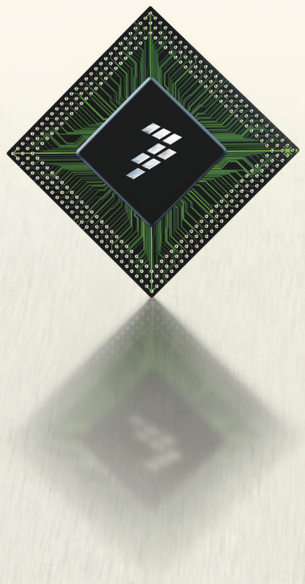

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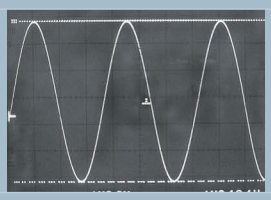

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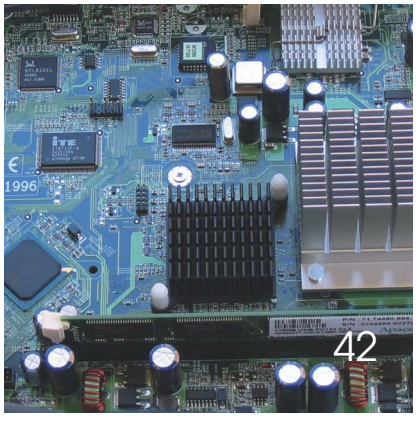

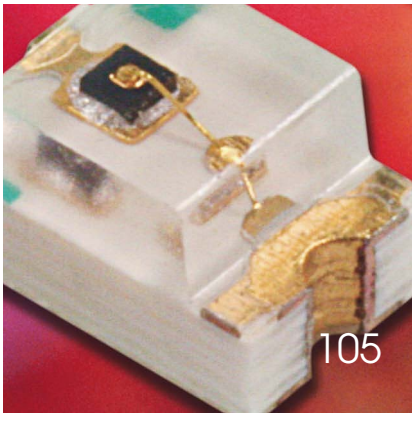

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Xilinx has added five Spartan 3E devices and a Virtex 4 device, which includes a hardwired PowerPC core, to its XA automotive FPGA lineup.
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Moore still explosive, 40 years after setting down the Law

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Satellite tuner targets PayTV market

Zarlink Semiconductor's ZL10037 suits standard- and high-definition satellite receivers in PayTV systems.
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ON THE VERGE

Proponents of power-line networking tend to sound more like Southern Baptist preachers than technologists. A video-enabled iPod makes no sense unless Apple also has a video version of its iTunes store up its sleeve. And the two competing high-definition DVD formats might actually coexist for years to come.

These excerpts are just a sampling of the opinions available at On the Verge, a blog devoted to digital consumer-electronics gadgets and the converged networks that feed them. Join Editor at Large Maury Wright and post your comments.
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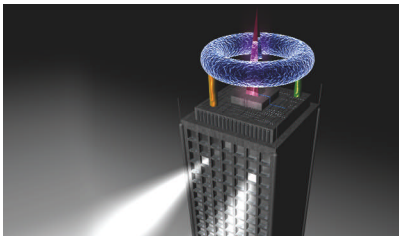

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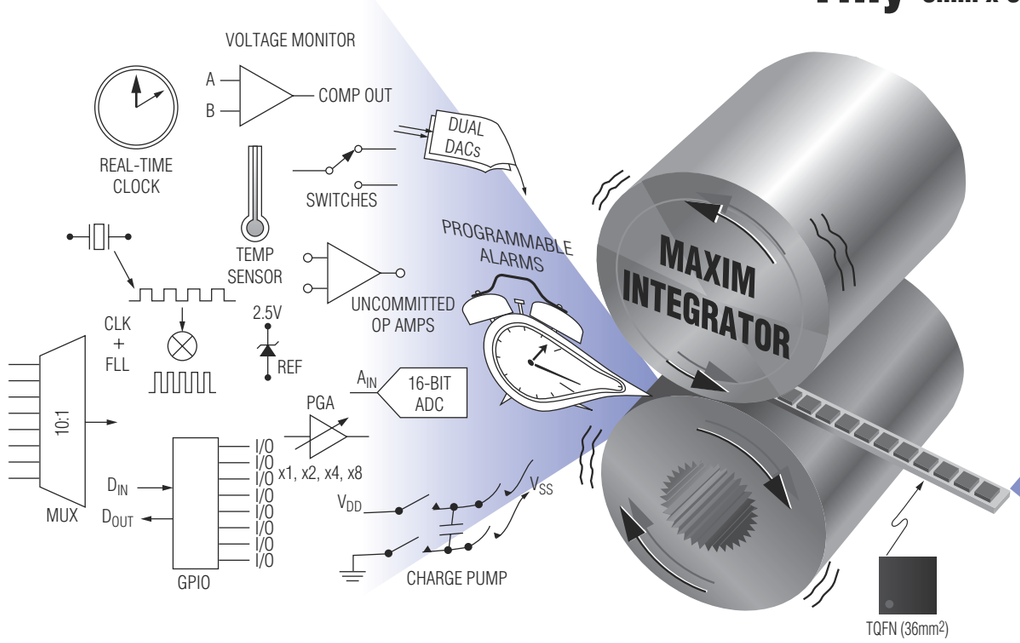

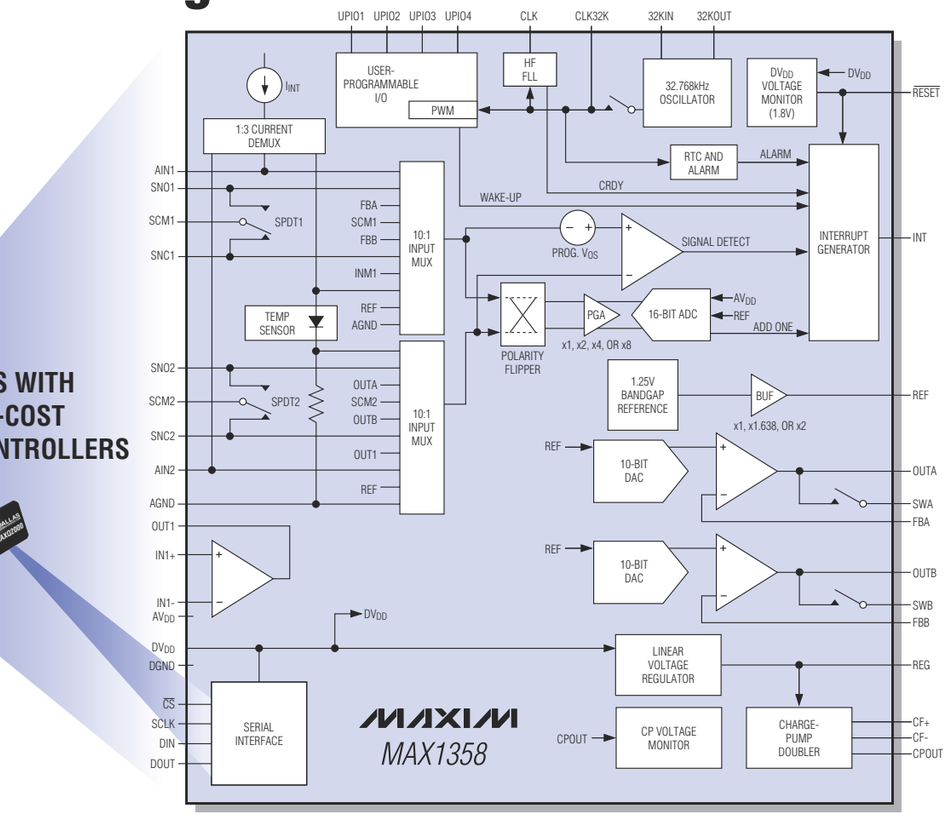

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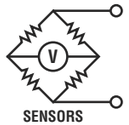

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BY BILL SCHWEBER, CONTRIBUTING TECHNICAL EDITOR

Does anybody really know what time it is?

Time is such a contradictory parameter. It is at the core of most scientific analysis and engineering design, we can measure and slice it with femtosecond precision, and we effortlessly take it for granted. After all, everyone knows what time—and *the* time—is. Yet, no one really understands it. Scientists and philosophers have for thousands of years debated its meaning (**Reference 1**). Can it go backward? Can you travel through time and, if so, change the past and thus the present and future? What does "now" mean? What does it even mean to say that time can slow down? When Einstein conjectured, as a consequence of his relativity theory, the now-proven fact that time does indeed slow down as you move faster, the time-related questions and answers became more puzzling.

Beyond the broad question of the meaning of time, a new problem with its definition is facing the scientific community (**Reference 2**). Atomic clocks at the NIST (National Institute of Standards and Technology, www.nist.gov) specify the legal and technical standard for the second (**Reference 3**). Yet, every few years, scientists must "correct" this definition because a second is also a fraction of the time it takes for the earth to rotate once on its axis: 24 hours equals 86,400 seconds. Because we can so precisely measure time and the Earth's position, we know that this rotation is slowing down due to the influence of the moon, global displacements, and other factors. The correction requires adding a leap second to official time to synchronize the atomic-clock-based time with global motion.

And that's the problem. Adding this leap second is neither trivial nor free of unintended consequences for systems that use precise clocks, especially embedded systems. Well-documented cases show that the leap-second addition causes large-scale system crashes, losses of synchronization, and many other problems. For these reasons, the United States has proposed to, by 2007, standardize the definition of a second as atomic, not astronomical. Over time, astronomical- and atomic-based time would diverge slightly, though enough to cause problems with precision applications.

The United States has proposed to, by 2007, standardize the definition of a second as atomic, not astronomical.

This seemingly simple proposal sparks controversy. The astronomy community points out that this change would make the tracking of heavenly motion and objects inaccurate. It would even adversely affect the tracking of launched satellites and guided missiles. The astronomy community has a deservedly large and historical presence at the ITU (International Telecommunications Union, www.itu.int). The ITU directs the IERS (International Earth Rotation and Reference Systems Service, www.iers.org). IERS, in turn, is the keeper of the official astronomical clock and defines Greenwich Mean Time. The ITU also tells the IERS what the change of definition for "second" should be and makes a strong case for the proponents of the change. Meanwhile, one could also make a strong case for the other view, which favors atomic-clock time.

No easy answer exists for resolving this issue. Both sides have good arguments. Our ability to precisely measure time, independently of the sky, conflicts with the measurements we make with our telescopes. One is neither better nor more correct, because how you view the conundrum depends on your perspective, definition, and application. Our tangible world of sun and sky clashes with the invisible world of atomic motion, which leads to some difficult and somewhat unsatisfactory decisions. Perhaps it's another manifestation of the conflict between our clock-driven schedules and a sunrise- and sunset-driven life (**Reference 4**).EDN

REFERENCES

1 *Scientific American*, September 2002.
2 Weinstein, Keith, "Why the US Wants to End the Link Between Time and Sun," *The Wall Street Journal*, July 29, 2005.
3 Israelsohn, Joshua, "How It Works: Time," *EDN*, March 15, 2001, pg 46, www.edn.com/article/CA75130.
4 Ellison, Harlan, "*Repent, Harlequin!" Said the Ticktockman*, Underwood Books, 1965.

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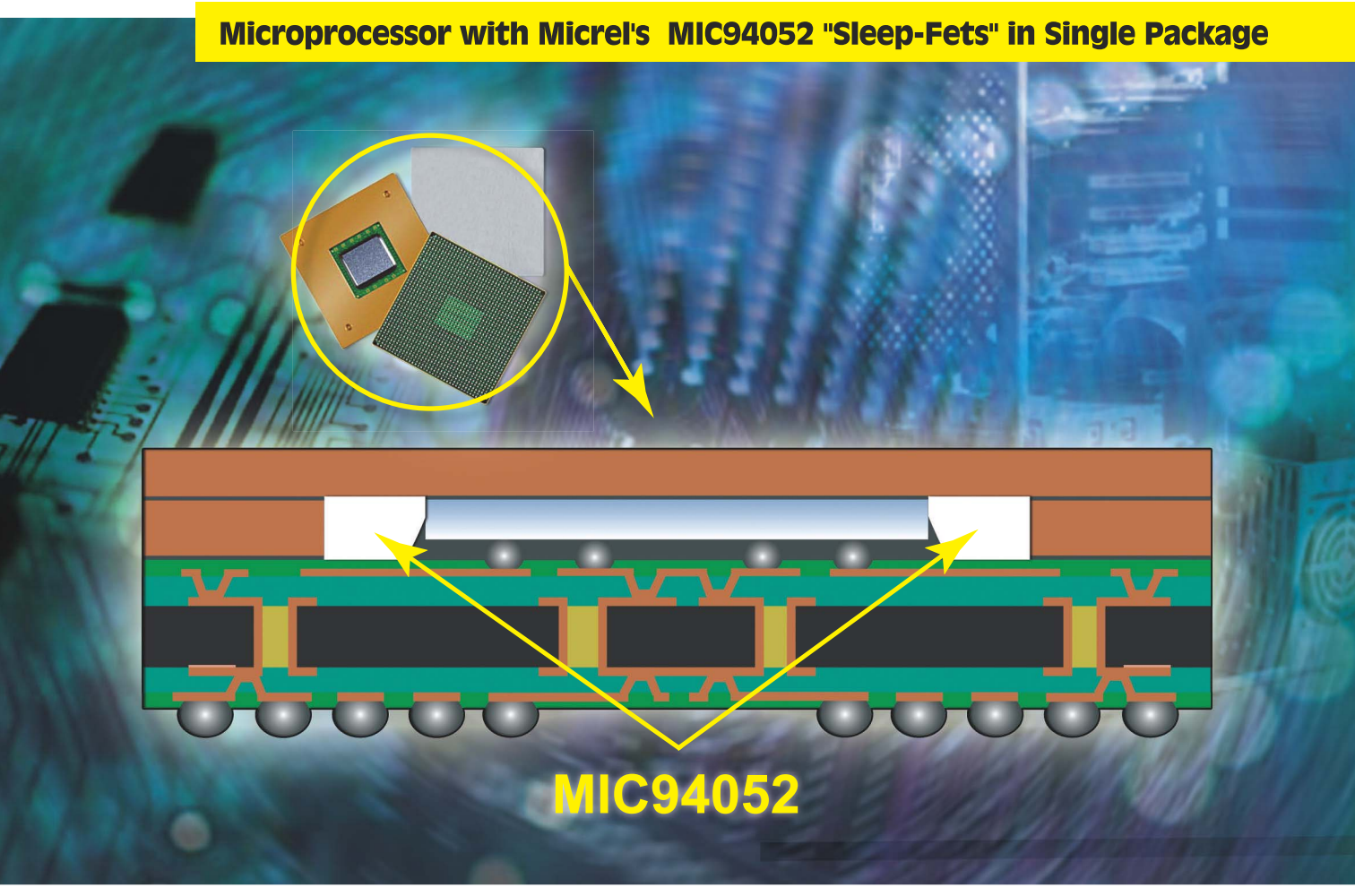
Rest Easy. Micrel's Sleep Transistor ICs are Low-Cost Solutions for Microprocessors



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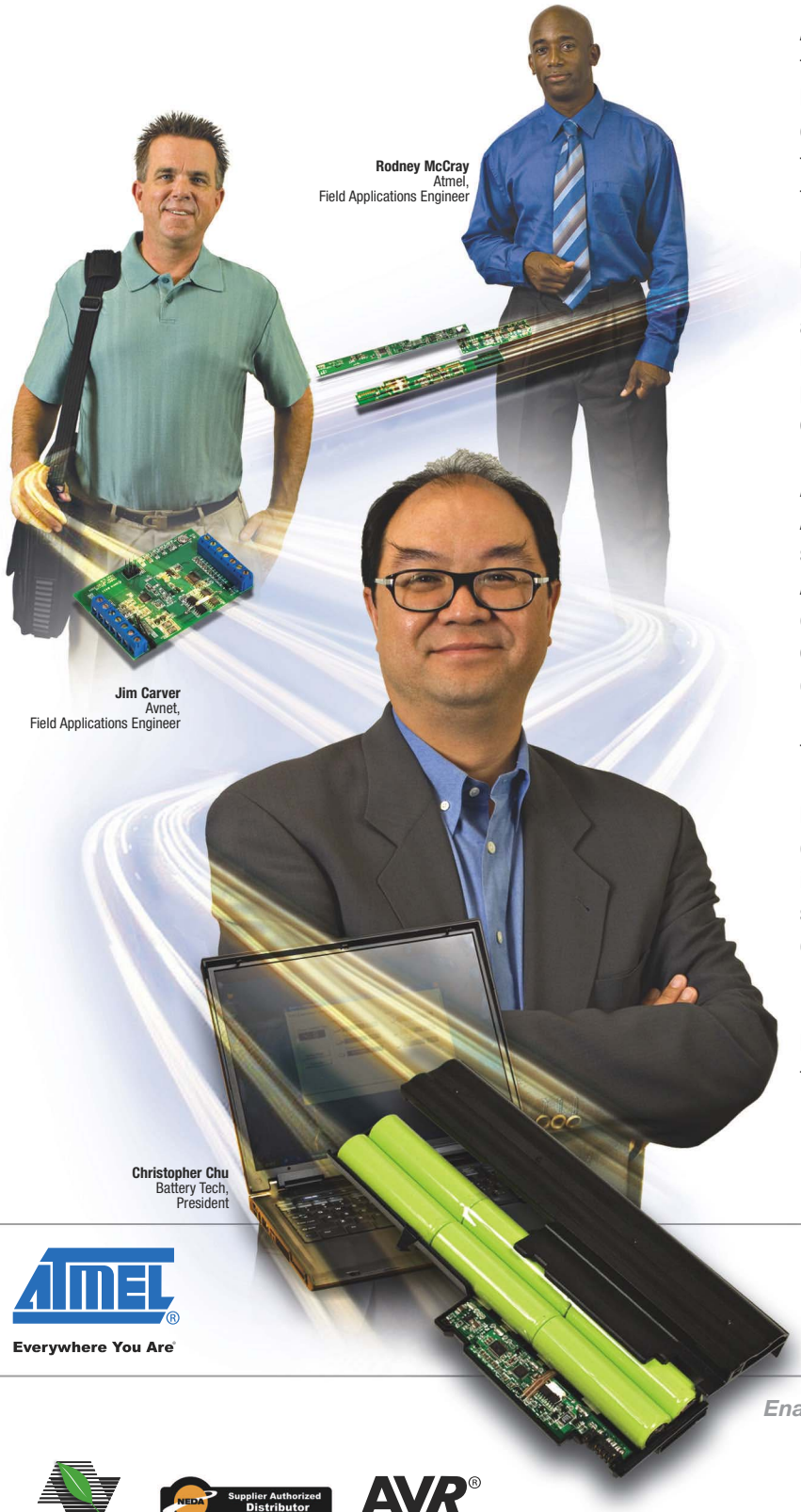
Avnet EM and Atmel – The Solution

Avnet's MCU specialist introduced a new product solution involving Atmel's 8-Bit Flash memory based AVR microcontroller that solved BTI's challenge quickly and efficiently. Today, BTI utilizes Avnet's point of use replenishment system (POURS) program to ensure the proper flow of components into the manufacturing line, as it readies these new products for volume production.

BTI has also charged Avnet and Atmel to move its existing designs to Atmel's AVR platform – the industry's leading flash-based microcontroller. It's no shock to see why – with Avnet and Atmel's focused energy, BTI found total support across the board.

For additional application solutions and to download the BTI case study, visit: www.em.avnet.com/atmel/satb



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No. 103

Understanding High-Speed Signals, Clocks, and Data Capture

— By Ian King, Applications Engineer

As today's data conversion sample rates for analog-to-digital converters are moving into the Giga Samples Per Second (GSPS) range, systems need to be capable of such high conversion rates and the supporting analog components have to generate and amplify high-frequency signals. In addition to the analog signal path, the circuit areas that the designer should thoroughly understand are the sampling clock and the capturing of digital data at high bit rates. This issue of the *Signal Path Designer* will provide suggested solutions for these two key areas. The following information is particularly relevant for systems that require high-performance ADCs.

Clock Sources

One of the most important sub-circuits within a high-speed data conversion system is the clock source. This is because the timing accuracy of the clock signal can directly affect the dynamic performance of the ADC. To minimize this influence, an ADC clock source must exhibit very low levels of timing jitter or phase noise. If this factor is not considered when choosing a clock circuit, the system could deliver poor dynamic performance irrespective of the quality of the front-end analog input circuitry or ADC. A perfect clock will always deliver edge transitions at precise time intervals. In practice, clock edges will arrive at continuously varying intervals. As a result of this timing uncertainty,

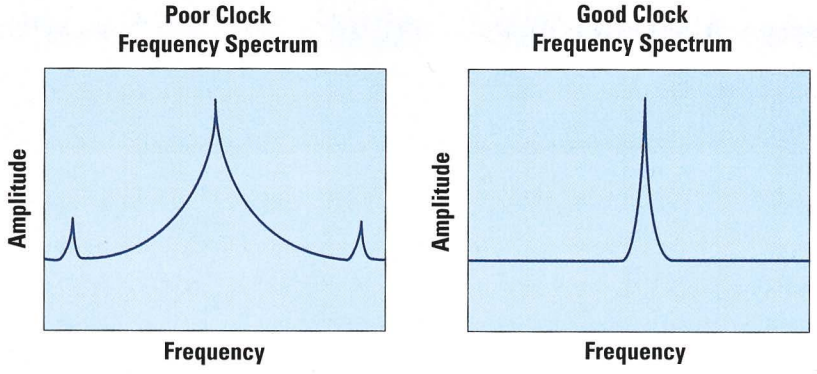


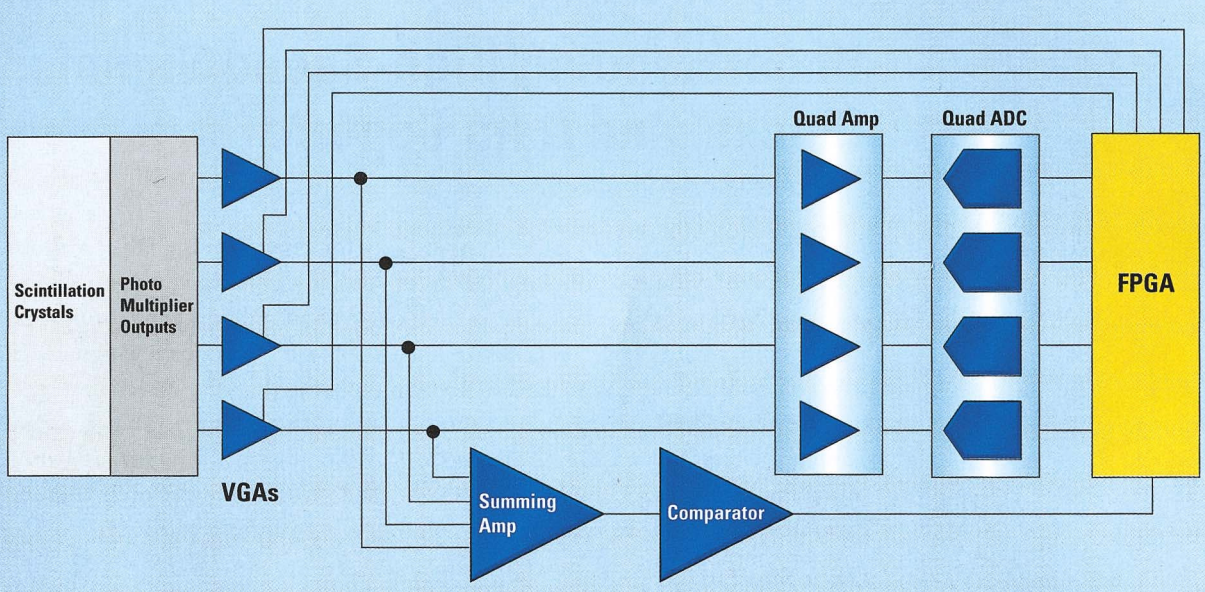
Figure 1. Examples of Clock Signal Spectral Analysis

NEXT ISSUE:
Precision Sensor Interface

National Semiconductor
The Sight & Sound of Information

High-Performance Solutions for Medical Imaging

Simplified Positron-Emission Tomography (PET) Scanner Block Diagram



High-Speed ADCs for Medical Imaging

						Dynamic Performance			
Product ID	Resolution	Speed (MSPS)	Supply Voltage (V)	Power (mW)	SFDR (dB)	THD (dB)	ENOB (bit)	SNR (dB)	Package
ADC10065	10 bit	65	3	68.4	80	-72	9.5	59	TSSOP-28
ADC10080	10 bit	80	3	78.6	79	-75	9.5	59	TSSOP-28
ADC10DL065	10-bit dual	65	3.3	360	80	-78	9.8	61	TQFP-64
NEW! ADC12DL040	12-bit dual	40	3	210	86	-83	11.1	69	TQFP-64
NEW! **ADC12DL065**	12-bit dual	65	3.3	360	86	-84	11.1	69	TQFP-64
NEW! ADC12QS065	12-bit quad	65	3	800	85	-83	11.0	69	TQFP-64, LLP-60
ADC14L020	14 bit	20	3.3	150	92	90	12.0	74	LQFP-32
ADC14L040	14 bit	40	3.3	236	90	87	11.9	73	LQFP-32

High-Speed Amplifiers and Comparators for Medical Imaging

Product ID	Type	SSBW (MHz, A_V = 1)	Slew Rate (V/µs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc, V_{OUT} = 2 V_{PP})	Voltage Noise (nV/√Hz)	Package
NEW! **LMH6550**	Fully differential ADC driver w/ disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6551**	Fully differential ADC driver	370	2400	12.5	-94 / -96 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6703**	1.2 GHz low distortion op amp w/shutdown	1.2 GHz[2]	4200[2]	11.0	-69 / -90 at 20 MHz, R_L=100Ω	2.3	SOIC-8, SOT23-6
LMH6502	Linear in dB, variable gain amplifier	130[1]	1800[1]	27.0	-55 / -57 at 20 MHz, R_L=100Ω	7.7	SOIC-14, TSSOP-14
LMH6503	Linear in V/V, variable gain amplifier	135[1]	1800[1]	37.0	-60 / -61 at 20 MHz, R_L=100Ω	6.6	SOIC-14, TSSOP-14
LMH6504	Linear in dB, variable gain amplifier	150[1]	1500[1]	11.0	-47 / -55 at 20 MHz, R_L=100Ω	4.4	SOIC-8, MSOP-8
LMH6722	Quad wideband, low power op amp	400	1800	5.6	-72 / -85 at 5 MHz, R_L=100Ω	3.4	SOIC-14
LMH6725	Quad, ultra low power op amp	370	600[2]	1.0	-65 / -63 at 5MHz, R_L=100Ω	4.3	SOIC-14, TSSOP-14

Product ID	Type	Response Time (ns)	Rise/ Fall Times	I_{CC} (mA/ch)	CMVR	Output Config	Package
LMV7219	7 ns, 2.7V to 5V comparator w/ RRO	7	1.3 ns	1.1	-0.2V to 3.8V	Push-pull	SC70-5, SOT23-5

[1] A_V = +10 [2] A_V = +2

Understanding High-Speed Signals...

the signal-to-noise ratio of a sampled waveform can be compromised by the data conversion process.

The maximum clock jitter that can be tolerated from all jitter sources before the noise due to jitter exceeds the quantization noise (1/2 LSB). This is defined from the following equation:

$$T_{j(rms)} = (V_{IN(p-p)} / V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{in}))$$

If the Input Voltage (V_{IN}) is optimized to equal the full scale range of the ADC (V_{INFSR}), then the jitter requirement becomes a factor of the ADC's resolution (N bits) and the input frequency being sampled (f_{in}).

For input frequencies up to the Nyquist rate (500 MHz for a 1 GSPS conversion rate), the total jitter requirement would be:

$$T_{j(rms)} = 1 \times (1/(2^{(8+1)} \times \pi \times 500 \times 10^6))$$

$$T_{j(rms)} = 1.2 \text{ ps}$$

This value represents the total jitter from all sources. A source of jitter that can be accounted for within the ADC device itself is called the aperture jitter. This is a timing uncertainty associated with the input sample and hold circuit of the device and should be considered when determining the maximum allowable clock jitter of the clock source.

$$\text{Clock Circuit Jitter} = \text{SQRT}\,(T_{j(rms)}^2 - (\text{ADC Aperture Jitter})^2)$$

Using the ADC08D1000 as an example, the aperture jitter is given in the datasheet as 0.4 ps, this value tightens the jitter specification for the ADC clock to ~1.1 ps.

However, simply matching an oscillator's performance data to the requirements specification may not be enough to obtain the expected result when used in the data conversion system. This is because frequency components that exist alongside the fundamental also play a significant role. It is therefore important to examine the clock signal with a spectrum analyzer and make sure that the energy associated with the fundamental frequency is not spread over too wide a range. Spurs that extend to higher frequencies may be visible and will also have a direct impact on jitter performance. ***Figure 1*** compares an example of a poor performance clock signal alongside the frequency spectrum that would be expected from a good, clean low-jitter clock source.

Figure 2 shows the recommended clock circuit for the ADC08D1000. It consists of a Phase Locked Loop (PLL) device (LMX2312) connected to a Vari-L Voltage Controlled Oscillator (VCO).

The PLL and VCO maintains the required signal to noise ratio (46 dB) for the ADC08D1000 product up to the Nyquist input frequency. The FFT plot in ***Figure 3*** shows the dynamic performance of the ADC when clocked at 1 GSPS

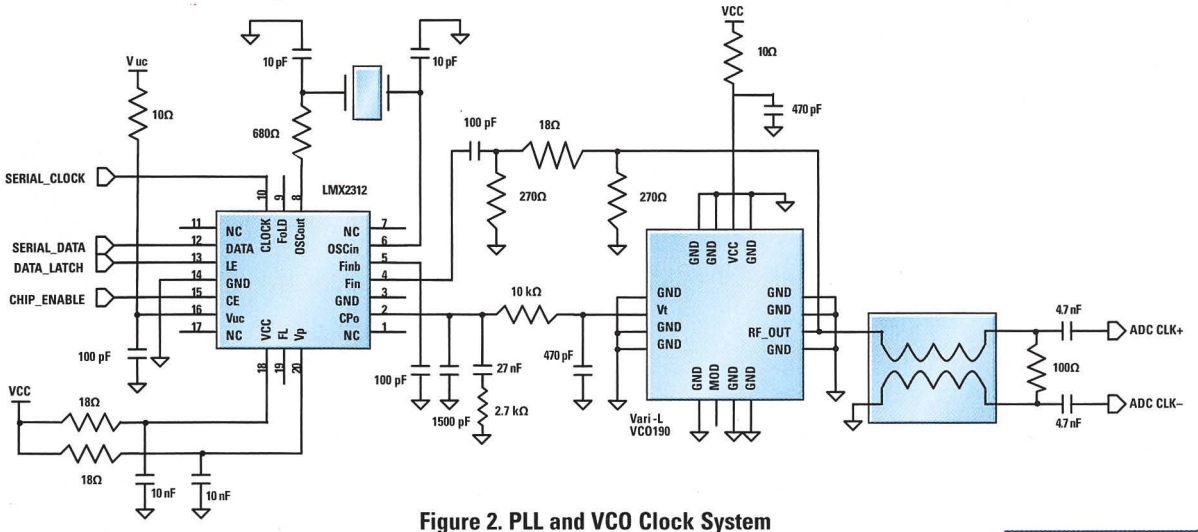
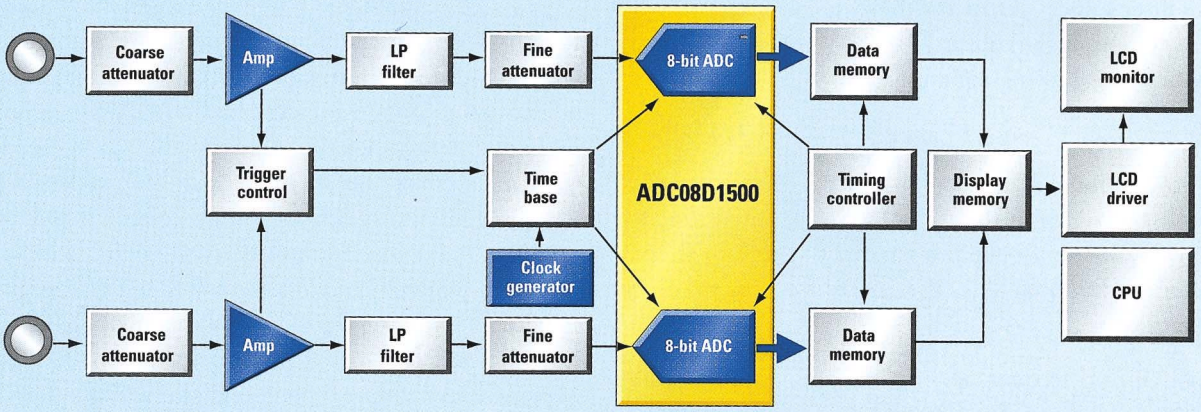


Figure 2. PLL and VCO Clock System

Signal-Path Solutions for Test and Measurement

Simplified Oscilloscope



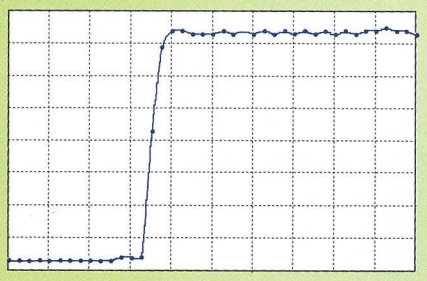
8-bit 1-3 GSPS ADC Family Performance (typical)

- 7.3 to 7.5 Effective Number of Bits (ENOB) at Nyquist
- 1.75 GHz full power bandwidth
- Bit error rate 10^{-18}
- DNL ±0.25 LSB
- Crosstalk -71 dB
- Operating power of only 1W to 1.8W (*no heat sink required*)

Features

- Interleaved dual-edge sampling (DES) mode enables up to 3.4 GSPS operation
- Choice of single or dual data rate output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control (gain, offset)
- Demultiplexed LVDS outputs simplify data capture

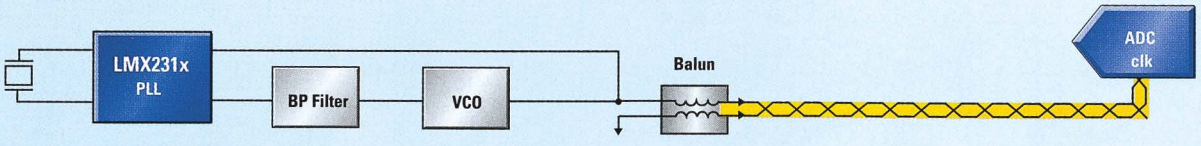
Step Response



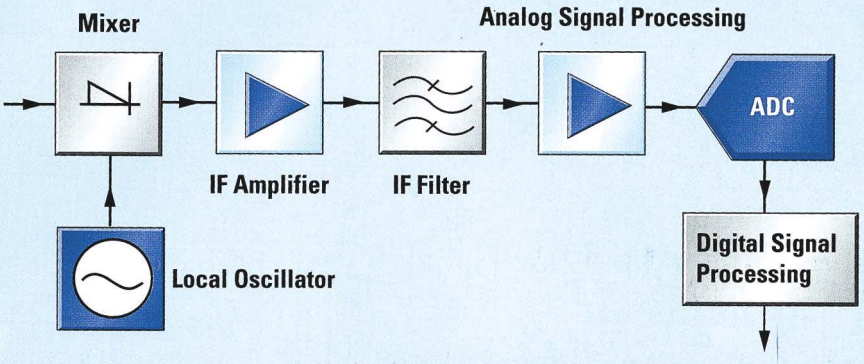
2 nS/div
I Input, 2 GSPS Interleaved Operation

Product ID	Description
ADC081000	8-Bit, 1 GSPS
ADC081500	**8-Bit, 1.5 GSPS**
ADC08D500	8-Bit, dual, 500 MSPS (1 GSPS in DES mode)
ADC08D1000	**8-Bit, dual, 1 GSPS (2 GSPS in DES mode)**
ADC08D1500	8-Bit, dual, 1.5 GSPS (3 GSPS in DES mode)

Clock Generator



Simplified Receiver Path



Applications:

- Spectrum analyzer
- Radar system
- Microwave links
- Wireless infrastructure

Local Oscillator PLLatinum™ Frequency Synthesizers

Product ID	Type	Frequency	Normalized Phase Noise	Phase Noise at Offset Frequency	Package
LMX2434	High Frequency Integer-N Dual PLL	1.0 - 5.0 GHz	-219 dBc/Hz	–	UTCSP-20, TSSOP-20
LMX2430	**Integer-N Dual PLL**	**0.2 - 3.0 GHz**	**-219 dBc/Hz**	**–**	**UTCSP-20, TSSOP-20**
LMX2470	Delta-Sigma Fractional-N PLL	0.5 - 2.6 GHz	-210 dBc/Hz	–	UTCSP-24
LMX2364	**Fractional-N PLL**	**0.5 - 2.6 GHz**	**-210 dBc/Hz**	**–**	**UTCSP-24, TSSOP-24**
LMX2347	Integer-N Single PLL	0.2 - 2.5 GHz	-217 dBc/Hz	–	CSP-16, TSSOP-16
LMX2512	**Frequency Synthesizer System with Integrated VCO**	**~ 1.0 GHz**	**–**	**-139 dBc/Hz at 900 kHz**	**LLP-28**

ADCs for Test and Measurement

					Dynamic Performance				
Product ID	Resolution	Speed (MSPS)	Supply Voltage (V)	Power (mW)	SFDR (dB)	THD (dB)	ENOB (bit)	SNR (dB)	Package
ADC08D1000	**8-bit dual**	**1000**	**1.9**	**1600**	**55**	**-55**	**7.4**	**47**	**LQFP-128 Exp. Pad**
NEW! ADC08D1500	8-bit dual	1500	1.9	1840	53	-53	7.3	46	LQFP-128 Exp. Pad
NEW! **ADC10DL065**	**10-bit dual**	**65**	**3.3**	**360**	**80**	**-78**	**9.8**	**61**	**TQFP-64**
ADC12L080	12 bit	80	3.3	425	80	-77	10.7	66	LQFP-32
NEW! **ADC12DL040**	**12-bit dual**	**40**	**3**	**210**	**86**	**-83**	**11.1**	**69**	**TQFP-64**
NEW! ADC12DL065	12-bit dual	65	3.3	360	86	-84	11.1	69	TQFP-64
NEW! **ADC12QS065**	**12-bit quad**	**65**	**3**	**800**	**85**	**-83**	**11.0**	**69**	**TQFP-64, LLP-60**
NEW! ADC14L040	14 bit	40	3.3	236	90	87	11.9	73	LQFP-32

Amplifiers and Comparators for Test and Measurement

Product ID	Type	SSBW (MHz, A_V = 1)	Slew Rate (V/µs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc, V_{OUT} = 2 V_{PP})	Voltage Noise (nV/√Hz)	Package
NEW! LMH6550	Fully differential ADC driver with disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6551**	**Fully differential ADC driver**	**370**	**2400**	**12.5**	**-94 / -96 at 5 MHz, R_L=800Ω**	**6.0**	**SOIC-8, MSOP-8**
LMH6702	Ultra-low distortion CFB op amp	1.7 GHz[1]	3100[1]	12.5	-100 / -96 at 5 MHz, R_L=100Ω	1.8	SOIC-8, SOT23-5
NEW! **LMH6703**	**1.2 GHz low distortion op amp w/shutdown**	**1.2 GHz[1]**	**4200[1]**	**11.0**	**-87/ -100 at 5 MHz, R_L=100Ω**	**2.3**	**SOIC-8, SOT23-6**
LMH6609	900 MHz, unity gain stable, VFB op amp	900	1400	7.0	-87 / -82 at 5 MHz, R_L=100Ω	3.1	SOIC-8, SOT23-5
LMH6574	**4:1 Mux, -70 dB crosstalk**	**500[1]**	**2200**	**13.0**	**-65 / -86 at 5 MHz, R_L=100Ω**	**5.0**	**SOIC-14**

Product ID	Type	Response Time (ns)	Rise/ Fall Times	I_{CC} (mA/ch)	CMVR	Output Config	Package
LMV7219	7 ns, 2.7V to 5V comparator w/ RRO	7	1.3 ns	1.1	-0.2V to 3.8V	Push-pull	SC70-5, SOT23-5

[1] A_V = +2

Understanding High-Speed Signals...

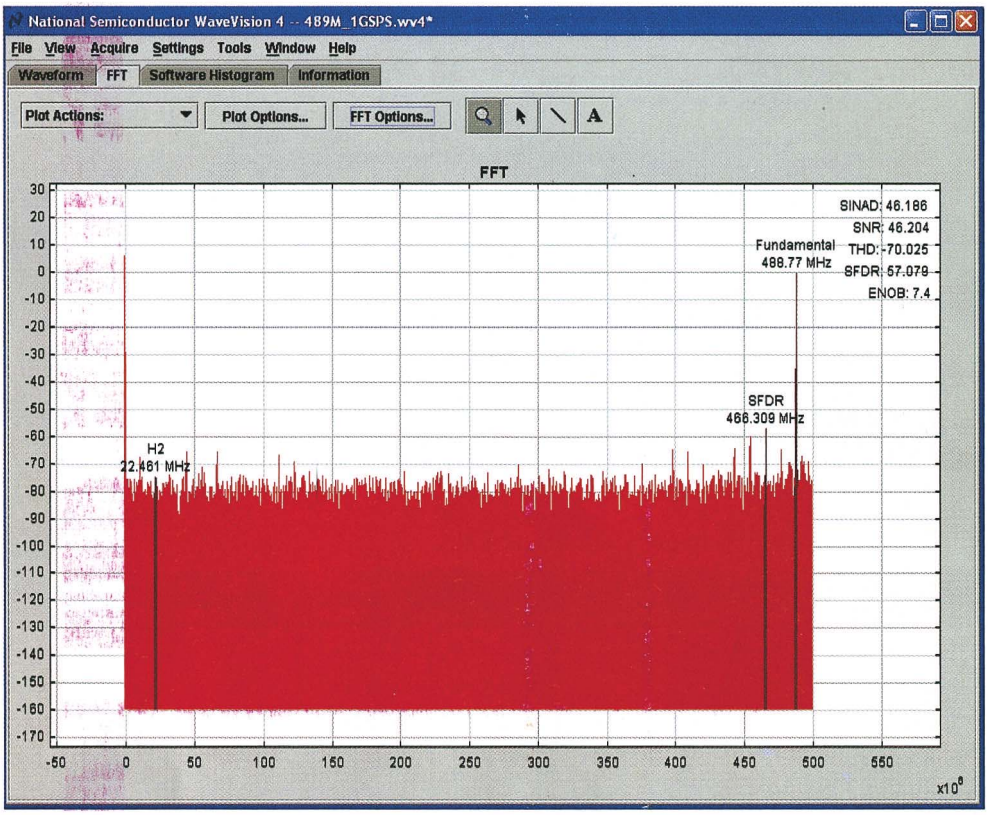


Figure 3. FFT Plot of a 489 MHz Sine Wave Sampled at 1 GSPS

using the circuit in *Figure 2* to sample an input frequency of 489 MHz.

Data Capture

Sampling signals at high frequencies (1 GSPS and above) means that the digital output data produced by the conversion has to be stored or at least transferred at very fast speeds. The two key issues when handling a billion conversions a second is that of signal integrity between the digital components in the system and also the rate of data transfer for each clock cycle.

To maximize the signal integrity of the digital outputs, high-speed ADCs use Low Voltage Differential Signaling or LVDS (see *Figure 4*).

The main advantage of the LVDS signaling method is that high data rates can be reached for a very low power budget. This is achieved through the use of 2 wires for each discrete signal that is to be carried across a circuit board or cable. The voltages on each of these conductors swing in opposite directions and also have a very small amplitude (typically 350 mV) when compared to single-ended signaling such as CMOS or TTL. It is because of the inherent noise immunity of the differential circuit that low voltage swings can be used. This in turn means that the signal frequency can be faster as the rise time is shorter.

The signal lines that carry the differential waveform on a circuit board should be designed to have a characteristic impedance of 100 Ohms (defined by the LVDS standard). These lines are then differentially terminated at the receiver with a 100 Ohm resistor to match the line. A signal voltage is generated across this 100 Ohm resistor by a 3.5 mA current source within the transmitter circuit which provides the 350 mV signal swing for the receiving circuit to detect.

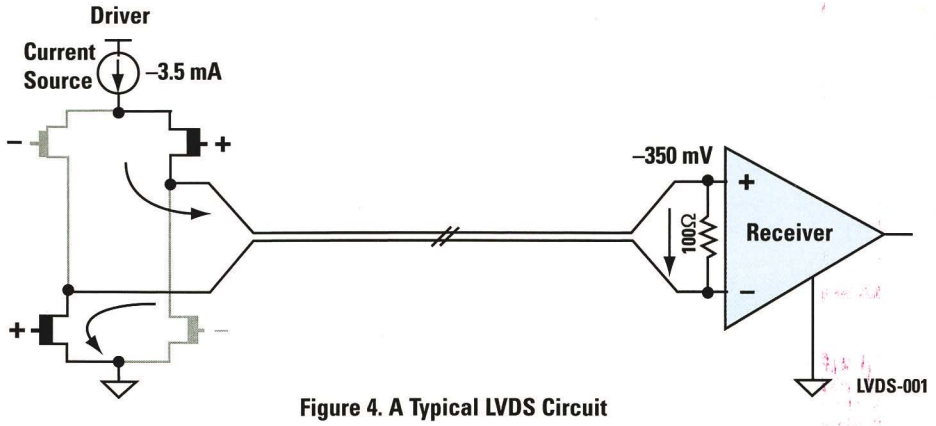


Figure 4. A Typical LVDS Circuit

Transmitting the data at high speeds is only half of the problem. Storing the data into a memory array for post processing is also to be considered. The ADC provides a de-multiplexed data output for each of its two channels. Instead of providing a single 8-bit bus running at a data rate equal to the sample rate, the device outputs two consecutive samples simultaneously on two 8-bit data buses. This method reduces the data rate by a half but increases the number of bits. For a 1 GSPS sample rate, the conversion data output from the ADC is 500 MHz. Even at this reduced speed, most discrete or internal FPGA memories would have problems capturing this data reliably. It is therefore beneficial to use a Dual Data Rate (DDR) method where data is presented to the outputs on both the rising and falling edges of the clock. While the data rate remains the same for DDR signaling, the clock frequency is halved again to a more manageable 250 MHz. This frequency is now in the realm of CMOS memory circuits. Before the data can be stored to memory, it requires an intermediate pair of data latches at the input to the FPGA device. The first latch of the pair is clocked using an in-phase data clock, while the second latch is clocked using a signal that is 180 degrees out of phase or an inverted data clock (see ***Figure 5***).

To simplify this clocking requirement, FPGAs come equipped with digital clock managers in the form of PLLs (Phase Locked Loop) or DLLs (Delay Locked Loop). These devices allow clock signals to be generated internally that are phase locked to an input clock, and offer phase delay taps of 0, 90, 180, and 270 degrees. This clock management feature allows a DDR clocking scheme to work effectively by providing a precise 180 degree phase-shifted clock. This in turn allows the incoming data synchronous to the falling edge to be captured reliably into a data latch.

After being latched, the incoming data can be transferred to a FIFO memory or Block RAM. From there the data can be easily retrieved by the system microcontroller at a much slower speed for post-capture processing.

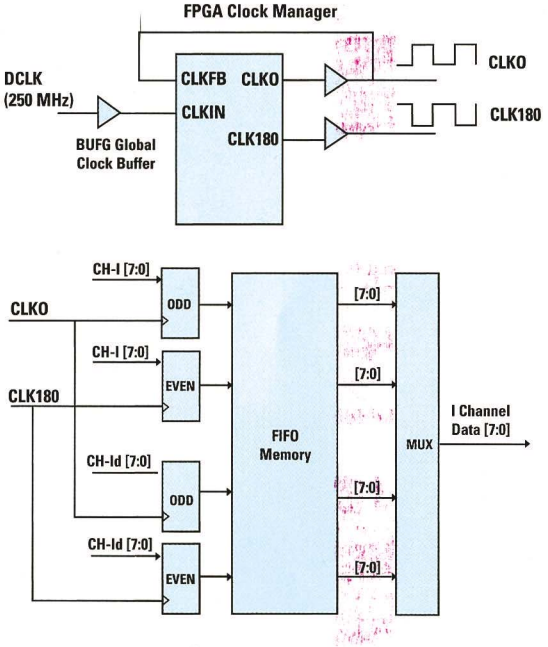


Figure 5. FPGA Data Capture Architecture

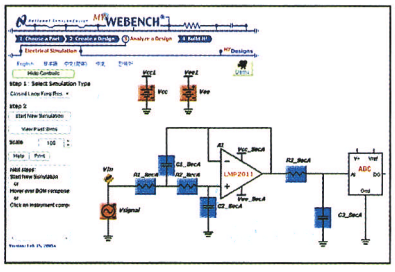
Summary

Ultra high-speed data conversion offers many challenges to the system designer. This is truly a mixed-signal environment in which all the sub circuits have to be considered carefully to allow the ADC to deliver the optimum dynamic performance. Clock systems that meet the low jitter requirements can be realized economically using off-the-shelf components. Similarly, FPGAs are available today with many supporting features for systems that include full LVDS support and clock management circuits. ■

Design Tools

INTRODUCING...

Signal-Path Design Tool



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Once you select a filter, it allows you to choose a matching ADC. Or, you can select an ADC first, then have the tool guide you to selecting the optimal filter to fit the ADC. This fast and easy tool allows you to select the best combination of components that are designed to work together and achieve your system goals for cost and performance.

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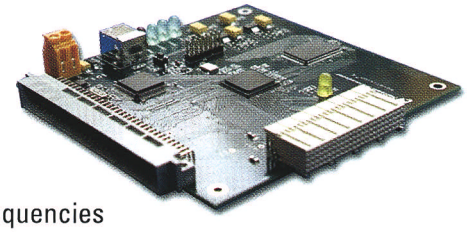
Test and evaluate A/D converters with National's easy-to use WaveVision 4.0 evaluation board. Each evaluation board comes complete with USB cable and support software.



Features and benefits:

- Plug-n-play ADC evaluation board
- USB interface to PC
- PC-based data capture
- Easy data capture and evaluation
- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
- Produces and displays FFT plots
- Dynamic performance parameter readout with FFT
- Produces and displays histograms

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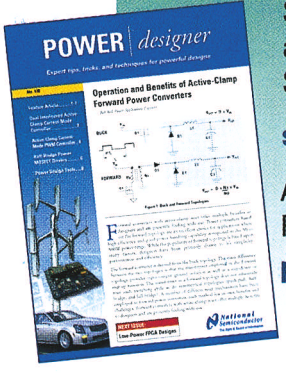

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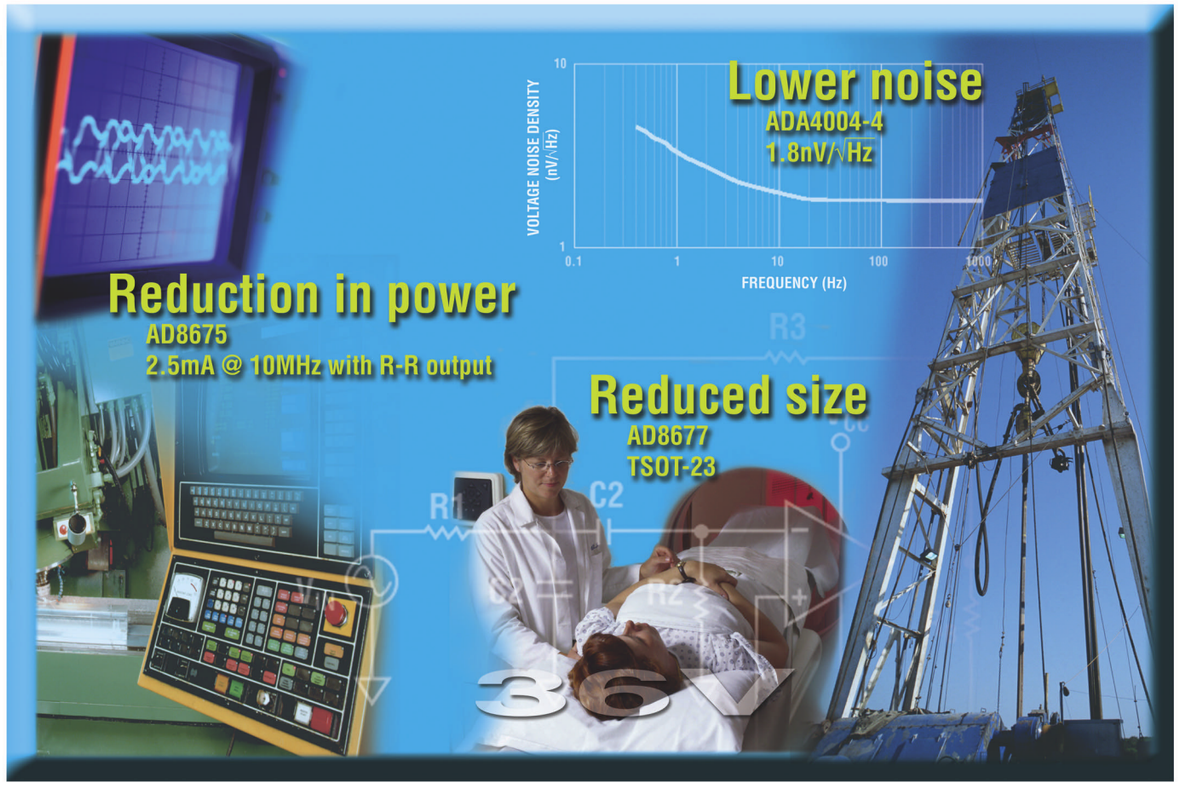

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Today's high voltage industrial designs are demanding more IC performance than ever. That's why Analog Devices has developed *i*Polar manufacturing process technology—the most significant re-engineering of high voltage bipolar technology in almost 20 years.

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Lowest noise in the smallest footprint

Our breakthrough manufacturing process yields analog ICs with superior noise and footprint characteristics. For example, the ADA4004-4 precision quad amplifier achieves 1.8 nV/√Hz voltage noise density—the industry's lowest wideband noise in this product category—while its 4 mm × 4 mm, 16-lead LFCSP occupies 70% less PCB area than the competition.

Superior speed and reduced power

*i*Polar technology enables a new generation of components that offer enhanced speed with markedly reduced power consumption. For example, at 10 MHz on 2.5 mA supply current, the AD8675 offers 20% higher bandwidth while consuming 50% less power compared to other high voltage ICs. Likewise, our ultralow offset voltage AD8677 operational amplifier reduces power consumption up to 40% without loss of bandwidth.

Solutions for all your high voltage needs

Our families of high voltage analog ICs are growing. Coming soon will be more *i*Polar devices—such as drivers, voltage references, and additional amplifiers, including new audio ICs. We're also expanding our line of amplifiers, converters, and mixed-signal ICs manufactured on our recently introduced *i*CMOS™ technology. Together these new processes offer state-of-the-art high voltage analog IC performance and value, and represent our ongoing commitment to industrial and instrumentation engineers. For more information, please visit our website.

AD8675
Low noise, rail-to-rail precision amplifier

- Low voltage noise: 2.8 nV/√Hz
- Rail-to-rail output swing
- Input bias current: 2 nA max
- Offset voltage: 75 μV max
- Offset drift: 0.6 μV/°C max
- Very high gain: 120 dB
- 3 mm × 4.9 mm, 8-lead MSOP
- Pricing: $1.17/1k quantities

AD8677
Ultralow offset voltage op amp

- Low offset voltage: 75 μV max
- Input offset drift: 1.2 μV/°C max
- Supply current: 1.2 mA
- High CMMR: 130 dB
- Dual supply operation: ±5 V to ±15 V
- 2.9 mm × 3 mm, 5-lead TSOT-23
- Pricing: $0.75/1k, quantities

ADA4004-4
Low noise, precision quad amplifier

- Low voltage noise: 1.8 nV/√Hz
- Wide bandwidth: 12 MHz
- Low offset voltage: 100 μV max
- Supply current: 1.7 mA/amp
- Dual supply operation: ±5 V to ±15 V
- Extended industrial temperature range −40°C to +125°C
- 4 mm × 4 mm, 16-lead LFCSP
- Pricing: $3.02/1k quantities

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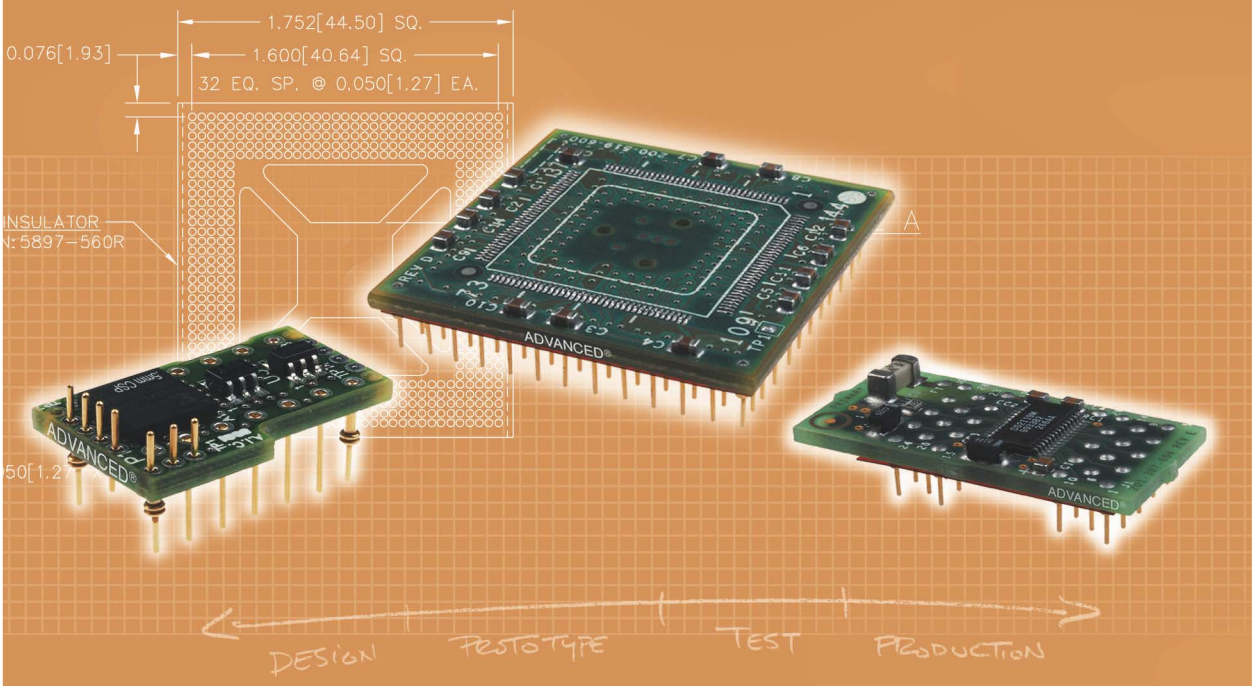
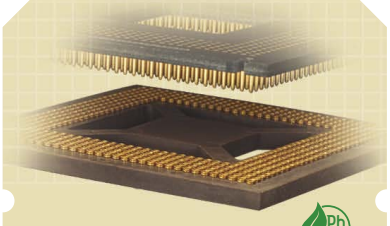


Don't redesign...Adapt.



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INNOVATIONS & INNOVATORS

We don't need no stinkin' RF-free room

Have it your way with the STE3000B benchtop RF-test enclosure.

"Personal" is the descriptive adjective for many devices, so why not a personal RF-test enclosure? If you have no access to or can't afford the preliminary sessions in a standard RF-screened room, consider a benchtop RF-test enclosure from Saelig Co. The unit's internal dimensions are 8 in. high, 17 in. wide, and 10.5 in. deep; it has ultrafine-shielded-mesh gloves in the access holes.

An RF-filtered supply powers internal illumination from low-voltage incandescent bulbs, letting users see through the RF-tight window and manipulate a product inside. The box comes with user-specified RF connectors for input and output. RF-absorbent foam with 24-dB attenuation lines the interior, and the double-sealed access-door lip has 90 dB of isolation. The STE3000B sells for $1095, approximately the price of a day's use of a commercial RF-screened room.**—by Bill Schweber**

▷**Saelig Co Inc**, www.saelig.com.

FERRITE-BEAD CHIP INDUCTORS STIFLE RF FLOW

Helping keep that pesky RF energy from propagating along signal lines where it doesn't belong, the CB series of multilayer ferrite-bead chip inductors from Stackpole Electronics is available in 0402 through 1812 case sizes. Depending on model, impedance ranges from 6 to 2700Ω with 20 or 25% tolerance. The devices target use in applications requiring 1 MHz to several hundred megahertz. The dc resistance is 0.02 to 1.2Ω, and current rating is 50 mA to 6A for these passive components, whose prices start at 5 cents (volume quantities).

—by Bill Schweber

▷**Stackpole Electronics**, www.seielect.com.

EDGE chip set offers multimedia features, slashes BOM

Although much of the hype in the handset business revolves around 3G standards, such as wideband CDMA (code-division multiple access), the bulk of the market is still in 2.5G standards, such as EDGE (enhanced data for GSM evolution). That fact led Agere to deliver the first member of its new Vision mobile-handset architecture in the EDGE flavor. The Vision X115 design seeks to maximize multimedia capabilities in a handset for mainstream customers and the 2.5G networks and do so in a way that Agere claims reduces cost by 20%. Mark Bode, director of product marketing, claims that the typical BOM (bill of materials) of an EDGE phone is in the low $50s for the ICs in the handset. Bode claims the X115 will reduce that BOM to the low- to mid-$40s.

Agere partitions the X115 design into digital- and analog-baseband ICs. The digital chip integrates three processing cores. An Agere DSP 16000 core is dedicated to PHY (physical)-level processing and the voice-codec tasks. An ARM 7 core is also dedicated to the EDGE function. An ARM 9 is available for applications and multimedia tasks, such as audio and video decoding.

The design supports dual color displays, including a primary QVGA or QCIF (Quarter Common Intermediate Format) display with 262,000 colors, as well as a 2 million-pixel camera for image input. The application processor enables playback of H.263 or H.264 (MPEG 4) video streams and MP3 or AAC (Advanced Audio Coding) audio streams. Bode claims that graphics performance is the other strong point of the design. The design attained a score of 350 in the independent JBenchmark 2.0 tests that essentially measure gaming performance. Bode claims that the 350 score places the design in the upper 10% of smart phones and PDAs tested and that Agere has yet to optimize the implementation that was tested.**—by Maury Wright**

▷**Agere Systems**, www.agere.com.

FEEDBACK LOOP

"Engineers love opening the box and poking at the insides to figure out what else can be done with the bits."

—George Gibson, in *EDN*'s Feedback Loop at www.edn.com/article/CA629314. Add your comments.

Broadband over coax plays both home- and access-networking roles

Entropic Communications is making good on its promises to use existing coaxial cables to deliver broadband data. The company focuses primarily on using the coax installed in most homes as a high-speed backbone for home networks that can distribute multiple HDTV streams. The company's c.Link technology allows communications through splitters, thereby working over the coax topologies in homes. Entropic officials believe that the c.Link technology can also deliver broadband services to homes or subscribers in MDUs (multiple-dwelling units). Entropic also led the development of the MoCA (Multimedia over Cable Alliance, www.mocalliance.org) industry group that has developed broadband-over-cable specifications.

Now, it appears that MoCA technology is ready for deployment. On the access side, Japanese MSO (multiple-system operator) J:Com (www.jcom.co/jp) will offer broadband services in MDUs using Panasonic (www.panasonic.com) gear that the company based on Entropic chips. J:Com will offer data services at speeds as high as 100 Mbps. The deployment relies on fiber to a building that connects to network controllers, which, in turn, can serve as many as 31 subscribers over installed coax plants.

On the home-networking front, Motorola (www.motorola.com) has developed a series of set-top boxes that it based on Entropic's technology. Motorola has also developed an HMA (home-media architecture) that it will offer MSOs to provide distributed PVR (personal-video-recording) functions throughout a home. The HMA supports a central PVR that can feed multiple low-cost set-top boxes in a home and also supports full PVR functions in multiple locations in a home. The HMA will rely on Entropic technology to move the video streams around the distributed topology.

Finally, the MoCA organization is also moving forward. Members include Cox Communications (www.cox.com), Motorola, Panasonic, RadioShack (www.radioshack.com), and other industry stalwarts. Other IC vendors, including Broadcom (www.broadcom.com), have also joined. The organization this year completed the MoCA spec and a round of field trials. Throughout the remainder of the year, the group is working on certification and expects certified products early in 2006.

—by Maury Wright

▷**Entropic Communications**, www.entropic.com.

FEEDBACK LOOP

"Unfortunately, the semiconductor people cannot solve all your problems in an elegant little chip, and a good, old-fashioned capacitor dielectric or iron or a battery must come to the rescue."

John K Fitch in *EDN*'s Feedback Loop at www.edn.com/article/CA608153. Add your comments.

Wireless-USB chip adds VOIP

For the past few years, Cypress has been pushing its proprietary WirelessUSB technology in applications ranging from HIDs (human-interface devices), such as wireless mice, to lightweight industrial control. The newest addition to the line, the WirelessUSB LP (CYRF6936), supports data rates as high as 1 Mbps, making the voice application feasible. But the WirelessUSB LP scheme also employs Cypress' Auto-Rate Receiver technology, which enables transfers at any speed with no need to negotiate a speed change.

An automatic transaction sequencer and 16-byte send and receive buffers allow designers to pair the WirelessUSB LP chip with low-cost microcontrollers. Moreover, the new chip can power external components, such as optical sensors. Production quantities are due in the first quarter of next year, and the devices will sell for as little as $1.20 (high volumes).

–by Maury Wright

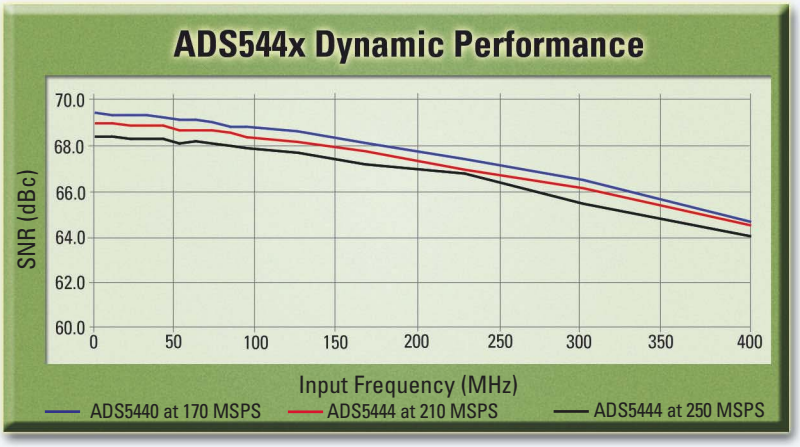
▶**Cypress Semiconductor**, www.cypress.com.

The WirelessUSB LP offers lower power and greater performance for VOIP wireless headsets.

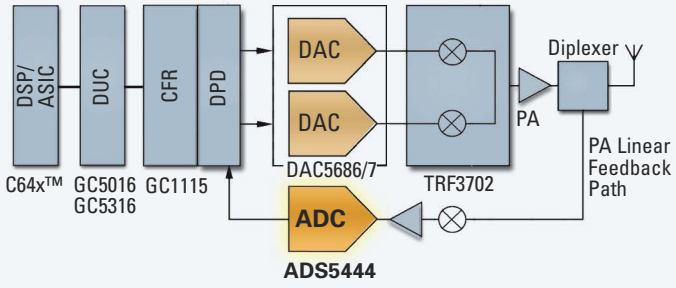
DILBERT *By Scott Adams*

High Speed, Top Performance!

13-Bit, 250-MSPS ADC



Sample Application: Wideband, High IF DPD Feedback Receiver



The new **ADS5444** from Texas Instruments sets a new benchmark for high-speed ADCs, providing best-in-class performance at 250 MHz. Look to TI for a complete portfolio of high-speed ADCs, including the recently announced ADS5440 13-bit, 250 MSPS ADC.

Device	Resolution (Bits)	Speed (MSPS)	SNR (dBc)	SFDR (dBc)
ADS5444	13	250	68 at 230 MHz IF	75 at 230 MHz IF
ADS5440	13	210	68 at 230 MHz IF	79 at 230 MHz IF
ADS5500	14	125	69.5 at 100 MHz IF	82 at 100 MHz IF
ADS5424	14	105	74 at 50 MHz IF	93 at 50 MHz IF
ADS5541	14	105	71 at 100 MHz IF	86 at 100 MHz IF
ADS5423	14	80	74 at 50 MHz IF	94 at 50 MHz IF
ADS5520	12	125	68.7 at 100 MHz IF	82 at 100 MHz IF
ADS5521	12	105	69 at 100 MHz IF	86 at 100 MHz IF

▶ Applications

- Software-defined radio
- Base stations:
  - Wideband receiver
  - High IF receiver
  - PA linearization
- Instrumentation
- Test and Measurement

▶ Features

- 100 MHz IF: SNR = 68.7 dBc; SFDR = 73 dBc
- 230 MHz IF: SNR = 68 dBc; SFDR = 75 dBc
- Fully buffered analog inputs
- 2.2 Vpp differential input voltage
- 3.3 V LVDS compatible outputs
- TQFP-80 PowerPAD™ package
- Industrial temperature range –40°C to +85°C
- Price: $95 1k

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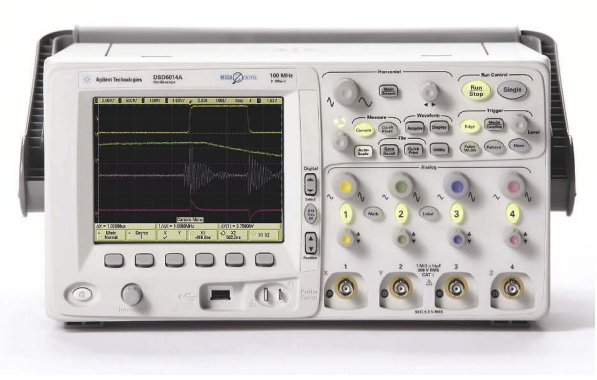
Texas Instruments

Midpriced, 100-MHz MSOs provide 16 digital and two or four analog channels

According to Johnnie Hancock, program manager for Agilent's moderately priced 6000-series MSO (mixed-signal oscilloscopes) and DSOs, the market for 100-MHz scopes is alive and more than just well. "Unit volumes at this bandwidth continue to exceed those of many wider bandwidth instruments, even though the higher performance products' steeper prices can yield greater revenues," he says. He also notes that Agilent's number-one scope competitor, Tektronix (www.tektronix.com), offers no MSOs like Agilent's, which combine 16 logic-timing-analysis channels with two or four analog channels. (Tek does, however, offer software that facilitates the use of its separate logic-analyzer instruments with its scopes.)

Agilent's number-two scope competitor, LeCroy (www.lecroy.com), offers a 32-channel logic-analysis accessory that you can add to several of its scopes, but, according to Hancock, the accessory approach doesn't provide the ease of use of the integrated approach that only Agilent and a third competitor, Yokogawa (www.yca.com), offer. Moreover, says Hancock, Agilent's customer studies show that MSO applications are mainly in development of embedded systems that use 8- or 16-bit microcontrollers. Few such applications call for more than 16 logic-analysis channels.

This product introduction adds 100-MHz MSOs and DSOs to a scope family that already includes units of both types with analog bandwidths of 300 MHz, 500 MHz, and 1 GHz. Like the 300-MHz units, the new 100-MHz units sample analog signals at a maximum rate of 2G samples/sec. (The maximum rate for the higher bandwidth units is 4G samples/sec.) A two-channel, 100-MHz DSO costs $4495. A four-channel, 100-MHz DSO costs $5595. Adding the MSO capability adds $2000. Users can in minutes easily upgrade a DSO to an MSO without using tools.



A large, covered compartment accessible from the top of the DSO6014 holds probes, other accessories, and even books that you might want for reference when you take the unit off-site.

Standard memory depth is 1M samples/analog channel. On any 100- or 300-MHz unit, regardless of the number of channels, users can double this depth for $500 or increase it to an 8M-sample/analog channel for $2000—also in minutes, without using tools. A 6000-series scope equipped with 8M-sample memory captures records 800 times as long as those that the most popular competitive scopes can capture. The 6000-series MegaZoom III display technology also enables you to quickly zoom in on waveform details within these long records. Moreover, according to Agilent, the display-update rate is as much as 40 times as fast as that of competitive instruments.

MSOs in the 6000 series fully support Agilent's FPGA dynamic probe, which the company introduced last year for use with its logic analyzers. The dynamic probe enables embedded-system developers to "see inside" Xilinx (www.xilinx.com) FPGAs and to correlate the internal view with events displayed on an MSO's analog and logic channels.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com.

Reference design adds support for mobile WiMax

WiMax news will be abundant in the near term as the WiMax World conference (www.wimaxworld.com) kicks off in Boston this week. Companies are getting a jump-start on the proceedings, rolling out new WiMax products. Sequans Communications (www.sequans.com) just announced its first WiMax SOCs (systems on chip) targeting both base-station and subscriber equipment. Meanwhile, picoChip moved to add mobile-WiMax support. The market leader in chips for the base-station side of the WiMax equation, picoChip just added support for the coming mobile flavor.

The picoChip PC102 adds support for 802.16e.

Although the fixed flavor of WiMax is starting to find success in places in which DSL or cable broadband don't prevail, the bigger opportunity for WiMax may be in the mobile flavor (see "WiMax wireless broadband: Fixed-flavor questions abound, mobile lurks," *EDN*, March 31, 2005, pg 44, www.edn.com/CA512128). Because the picoChip PC102 that WiMax base stations use is essentially a programmable DSP, the company has been able to add support for 802.16e and the Korean-developed WiBro mobile flavor through changes in the software stack. The result is a new PC6530 reference design and perhaps the first shipping support for mobile WiMax.

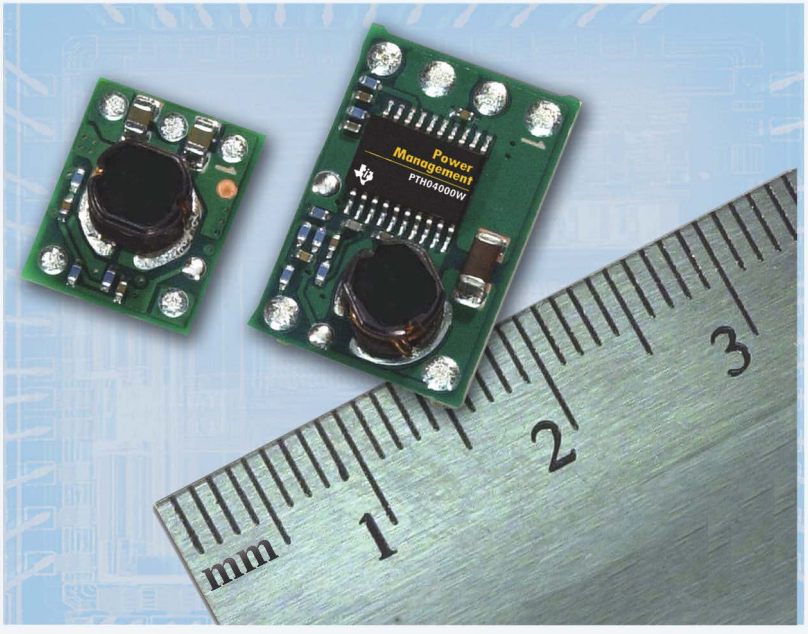
—by Maury Wright

▷**picoChip**, www.picochip.com.

POWER MANAGEMENT

Tiny 3-A Plug-In Power Modules

Achieve 94% Efficiency



▸ Applications

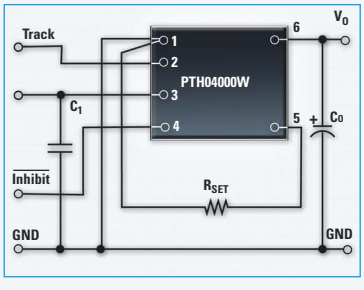
- Networking
- Servers
- Data communications
- Workstations
- Industrial electronics

▸ Features

- Auto-Track™ Sequencing
- Wide range of input voltages-3V to 5.5V or 4.5V to 16V
- 94% efficiency
- POLA™ compatible
- Under-voltage lockout
- Pb-free

Though tiny in size, the **3-A POL power modules** from Texas Instruments are packed with big features. At virtually the same size as a TO-220 package, these products can be used with input voltages from 3 V to 14 V and will provide output voltages from 0.9 V to 5.5 V. They are available with and without Auto-Track sequencing and all models include on/off inhibit control, over-current and over-temperature protection.

Device	I_{OUT} (A)	V_{IN} Range (V)	V_{OUT} Range (V)	Auto-Track Sequencing	UVLO	POLA	On/Off Inhibit	Over-Current	Over-Temp	Size (mm)
PTH04070W	3.00	3.0 to 5.5	0.9 to 3.6				X	X	X	13 x 10
PTH08080W	2.25	4.5 to 18	0.9 to 5.5		X		X	X	X	13 x 15
PTH04000W	3.00	3.0 to 5.5	0.9 to 3.6	X		X	X	X	X	13 x 19
PTH08000W	2.25	4.5 to 14	0.9 to 5.5	X	X	X	X	X	X	13 x 19



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Q&A

Kris Pister

Don't bother vacuuming this smart dust.

The inventor of Smart Dust and a longtime leader in the academic wireless-sensor-networking community, Kris Pister in 2002 co-founded Dust Networks to deliver his vision of a commercially robust wireless-sensor-networking platform. Pister is the chief architect of Dust Networks' patent-pending SmartMesh technology. Previously, he successfully commercialized or licensed micromachine technologies with Tanner Research, OMM Inc, Xactix, and Sony. He holds a doctorate and a master's degree in electrical engineering and computer sciences from the University of California—Berkeley and a bachelor's degree in science from the University of California—San Diego. Currently on leave as a professor of electrical engineering and computer science at UC Berkeley—and the father of four brilliant children—he is doing his part to continue the advancement of technology in the next generations.

How do you view the position of RFID and of smart sensors?

A RFID has lots of interesting applications. When people think of RFID, they think they know where their stuff is all the time, but all they really know is where it was when they last checked. That may work for FedEx, but not for the "where-is-it-right-now?" questions that many companies have for their critical machinery or perimeter-security systems.

There's a lot of stuff going on in wireless-sensor networks that is headed in that direction, as we drive costs down. There'll be true location capability—not in a decade, not in three months, but perhaps in three years. Our wireless-sensor networks gather information other than location from the physical world. Our networks can sense things, such as temperature, light, motion, and vibration.

For all the sensors out there, the wiring cost is tremendous. Step One: Do them wirelessly. Step Two: costs are down; put in more sensors. Step Three: Now that you have wireless sensors, put them in new places, on things that move around. It's not a killer app, but there will be a lot of happy applications and tremendous return on investment in commercial and industrial settings.

What about the relationship between the university and technology development?

A The easiest way to move technology from the university is to find a killer app. But if the story is different—less dramatic—it is much harder to do that.

What is your view on engineering education and students?

A I teach graduate and undergraduate courses at Berkeley. Students have a certain lack of "hardware dabbling." It's harder and harder for a kid in high school to play with circuits. But, if they order a [Microchip] PIC-design kit, they get an 8-bit microprocessor and setup for little money, and can do some real work. Otherwise, early on, they are forced to make the jump to abstraction and away from the physical world.

How does the decline of the big corporate R&D labs affect your research?

A I always try to work on stuff at least a generation ahead of the labs; that's where the fun is, where people don't think it's possible. I can guess where things are headed, but people in academia can easily fool themselves into solving problems that people don't have.

How do you deal with intellectual property you develop in a public-university setting?

A Any time that you have IP and money at stake, people complain. The EE/CS department at Berkeley has a culture of sharing, putting everything in the public domain. We generally don't patent things. There are good arguments for doing this, but there is also a good case to be made for the reverse.

What about working with venture capitalists?

A If people had loaned me money with no strings attached, we'd be worse off. I learned a lot of painful lessons.

What changes would you like to see in engineering education?

A I would like to see some more basic, early experiments in engineering. We shove students through a lot of math, basic physics, and similar before they get to do fun experiments. I'd like to run a course based on a book called something like "Dangerous Experiments in Electricity." Doing cool stuff in a controlled environment at the university would be good for them.

—by Bill Schweber

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Caveat Emptor!

Q. *How do I make sense out of a data sheet?*

A. With some difficulty. The ostensible purpose of a data sheet is to provide the user and potential user with the fullest possible information about the functions and technical characteristics of the device concerned. But the realities practically ensure that there are too many cooks concocting these documents, producing spoiled broth indeed.

The IC designer who writes the first draft wants to emphasize the genius of his or her creation. The marketing manager wants to stress competitive advantages while soft-peddling any drawbacks. The test engineer wants to minimize the time and cost of production testing, and tries to remove all maxima and minima from the table of characteristics, instead replacing them with "typical" values. Corporation lawyers want to make certain that potential (mis)users of the device have no grounds for suing the Corporation. Corporate communications wants the document shrunk from 60 pages to four. And applications engineers (ahem!) want the data sheet so clear and simple that even a software engineer can understand it and they can sleep away their afternoons without the applications enquiry phone ringing. The final product is a "compromise", and not always as helpful as it could be. And because data sheets are always produced in a hurry when the product is ready for release they always have some mistakes.

What's an engineer to do? First, know which specifications are most important to your application. If you don't know, consult design guides or screw up your courage and ask someone. Second, conduct parametric searches among manufacturers to find candidate devices. Third, despite your misgivings, read the d***ed data sheets. (I really did once have someone call to ask how many pins there are on an 8 lead mini-DIP.)

When reading data sheets, at the very least watch out for:

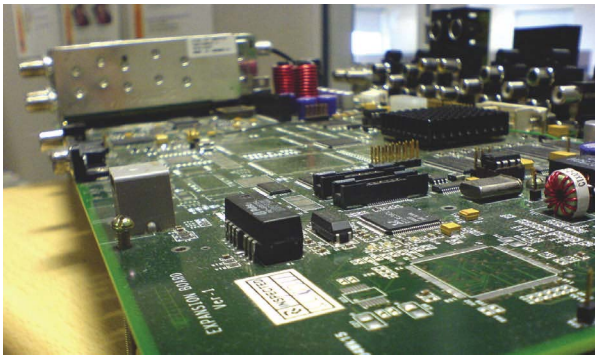
- "$V_{dd} \geq V_{ss}$" or, better "$|V_{ss}| \leq V_{dd}$" These are subtle ways of saying that if you supply the negative supply before the positive, the device will destroy itself.
- Specifications which appear similar on two data sheets but are not—such as small-signal bandwidth versus full-power bandwidth, or settling time to 1 lsb (12-bits) versus settling time to 1 percent.
- "Typical" versus maximum and minimum specifications. The meaning of maximum and minimum is clear and well-understood. The meaning of typical is open to many interpretations.

The "compromises" involved in meeting a data sheet's conflicting requirements mean that much more can be learned from a data sheet than simply the overt facts and specifications. The website below analyzes these things in considerable detail. It would be a wonderful thing if the industry could agree on a standardized format for data sheets and they all told the truth, the whole truth, and nothing but the truth. But I'm not holding my breath until it happens. Caveat emptor!

To learn more about how to read data sheets, Go to: http://rbi.ims.ca/4399-501

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com



Wipro Technologies has produced an HDTV receiver board for digital and rear-projection televisions.

GLOBAL DESIGNER

Digital TV comes with "India inside"

As HDTV in the United States and Europe gains traction, demand from consumer-electronics manufacturers for tuner and set-top-box chip sets is growing. Among the key suppliers to this industry is Broadcom. A number of leading television and set-top-box manufacturers, including Motorola (www.motorola.com), Echostar (www.dishnetwork.com), DirecTV (www.directv.com), Sony (www.sony.com), Pioneer (www.pioneerelectronics.com), Tivo (www.tivo.com), and Pace Micro Technology (www.pacemicro.com), use Broadcom chip sets.

The company's India development center has contributed to the design and development of several SOC (system-on-chip) designs for HDTV set-top boxes. According to Rajendra Kumar Khare, managing director of Broadcom India, his team was among the first to develop MPEG-2 HDTV decoders. "The India center has filed more than 130 US patents, many of them related to HDTV technologies," says Khare.

Meanwhile, MindTree Consulting (Bangalore) is designing a digital PVR (personal-video-recording) platform that can record and process HDTV and digital-TV streams. Because HDTV programming occupies a lot of disk space, the company is devising compression algorithms and building applications for electronic programming, detecting commercials, pausing, and resuming live video, says S Janakiraman, the company's president and chief executive officer for R&D services. The company is also creating combination devices that fuse a DVD player and a set-top box and is working on ultrawideband blocks that will enable wireless recording from an HDTV to a PVR device. MindTree plans to add support for BluRay-disk format in the PVR platform. "We are also working on devices that can convert from DVB-S to IP [Internet Protocol] for IPTV applications," says Janakiraman.

India's embedded-system-design leader, Wipro Technologies, has produced an HDTV receiver board for digital TV and rear-projection TV. An unnamed US manufacturer commissioned the company to design and develop a decoder board that would receive and decode the digital-broadcast signals and pass them on to a display board. Wipro created a multichip, multiboard architecture. Because the customer supplied the display board, the principal challenge was to implement a board-control protocol that provided comprehensive command and control semantics for multiboard communication. "We had to work with multiple peripheral-chipset providers to integrate their reference technologies onto the production software—and ensure that they worked seamlessly," explains Narayan Shenoy, group head of the Consumer Electronics Group at Wipro Technologies.

—by Chitra Giridhar, *EDN Asia*

▷**Broadcom**, www.broadcom.com.
▷**MindTree Consulting**, www.mindtree.com.
▷**Wipro Technologies**, www.wipro.com.

BITS AND PIECES

▷**Members of two England-based engineering institutions,** the IEE (Institution of Electrical Engineers) and the IIE (Institution of Incorporated Engineers), have established a new organization, dubbed the IET (Institute of Engineering and Technology), which will become effective early next year. For more, see www.edn.com/051027p1.

▷**South Korean cellular provider SK Telecom** has rolled out a digital smart-home service, with help from ZigBee-technology developer Ember, which it says will allow people to remotely control and monitor their homes using cell phones and the Internet. For more, see www.edn.com/051027p2.

10.27.05

Video-processing chip gets MII approval

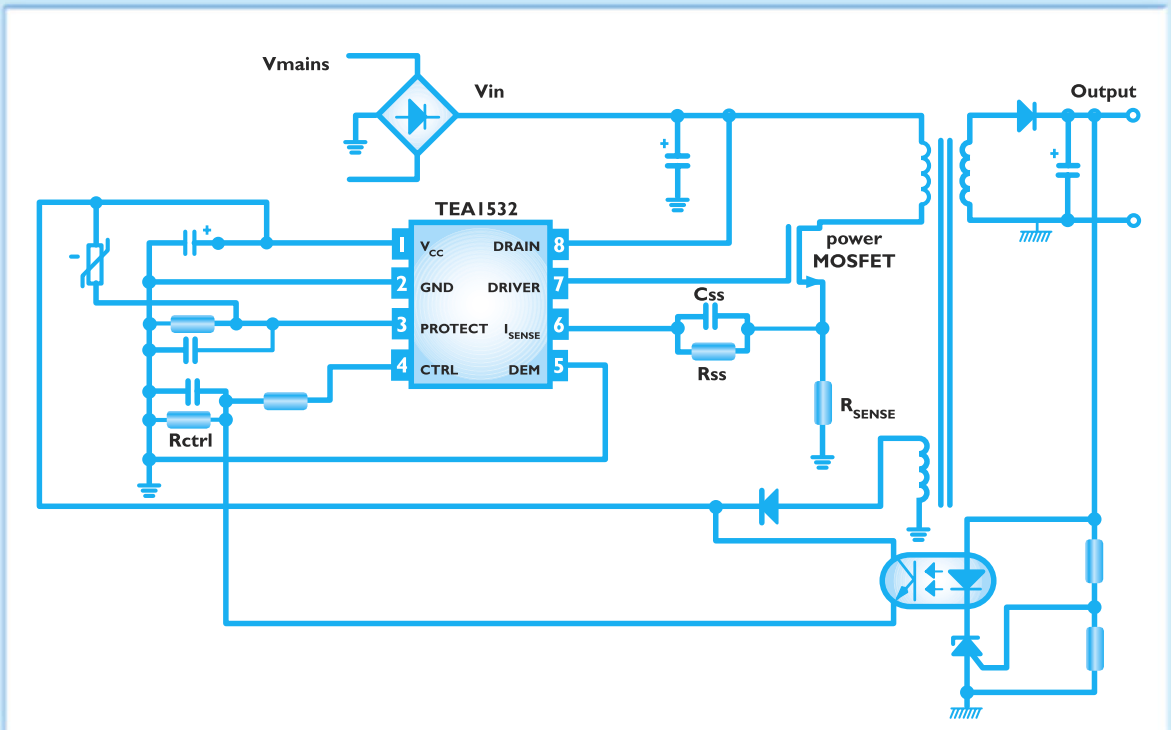
Hisense recently unveiled the Hiview digital-video media-processing chip, which successfully passed authoritative appraisal by the MII (Ministry of Information Industry). Hisense built the chip on a 0.18-micron CMOS process. It integrates almost 2 million logic gates and more than 7 million interior transistors. Hisense has been developing the chip over the last four years at its ASIC-design center. The company's Shanghai-based R&D team made the tape-out chip, which involved an investment of about 30 million yuan (about $37 million). Designers can use the product in various kinds of flat TVs, CRTs, and rear-projection TVs.

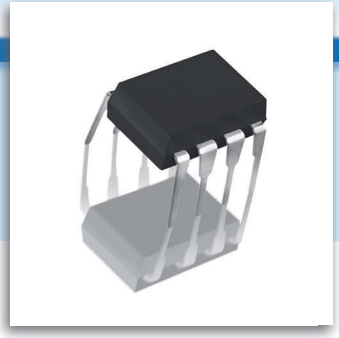
Hisense currently sells about 7 million TV sets per year. The company plans to use Hiview for digital high-definition TVs, with an expected production capacity of 1 million pieces this year. According to industry insiders, Hiview is not a pioneer product in China, but it may become one of the first video-processing chips to be commercialized.

—by Yao Gang, *EDN China*

▶**Hisense**, www.hisense.com.

GreenChip II





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BY BONNIE BAKER

Ease into the flexible CAN bus

When you need to select a network protocol, there are more choices than you may want. CAN (controller-area network) is one choice if you have a wired network. CANs have been around for more than 15 years. Historically, this bus targeted the automotive industry, because the bus provides predictable, error-free communications. Recent falling prices of CAN-system technologies make CANs commodity items. The CAN has expanded beyond automotive applications, migrating into systems such as industrial networks, medical equipment, railway signaling, and building-service controls. These applications use the CAN not only for its lower prices, but also because the communication you can accomplish through this network is robust, with a bit rate as high as 1 Mbps.

A CAN features a multimaster system that broadcasts transmissions to all system nodes. In this type of network, each node filters unwanted messages. A classic client/server network, such as Ethernet, relies on network addressing to deliver data to a single node. With multiple nodes in an Ethernet network, a star configuration implements centralized control (**Figure 1**). Although you need fewer microcontrollers to perform the varied tasks in an Ethernet system, the microcontrollers are usually more complex, with higher pin counts.

In contrast, every node in a CAN system receives the same data at the same time. By default, CAN is message-based, rather than address-based. The system integrates multiple nodes that use distributed control. With this topology, you can easily add or remove a node with minimal software impact. The CAN does require intelligence on each node, but you can tailor the level of intelligence to the task at that node. Consequently, these individual controllers are simpler, with lower pin counts. In addition, the reliability of the distributed-intelligence system is higher, with fewer wires.

Ethernet also differs from CAN in that Ethernet uses collision detection at the end of each transmission. CAN, on the other hand, uses collision recovery. When a collision occurs between two or more CAN nodes that transmit at the same time, the nodes with the lower priority messages detect the collision. The lower priority nodes then switch to a receiver and wait for the next bus idle to again attempt transmission. The winning transmitter continues sending its message as if nothing happened. Therefore, response time to collision correction is faster, because the correction occurs at the beginning of the message transmission. This structure prevents the destruction of higher priority messages.

The CAN specification, which Robert Bosch GmbH wrote, is standardized by ISO (International Organization for Standardization, ISO 11898) and SAE (Society of Automotive Engineers). This serial-communications protocol supports distributed real-time control with a sophisticated level of security. CAN's time-proven performance guarantees predictable, error-free communications for safety-conscious application. Through arbitration, CAN prioritizes messages with predictable latency times. The configuration is flexible at the hardware and data-link layers, at which designers modify transmission details. They do this modification while keeping system-wide data consistency. EDN

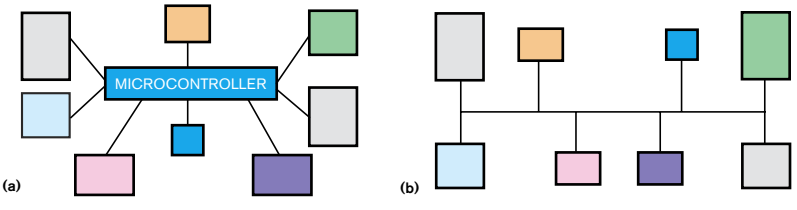

Figure 1 Multitask Ethernet-system networks employ a centralized topology (a). Adding a node to this system requires significant microcontroller modifications. With controller-area networks, using a distributed network means easily adding or removing of nodes, with minimal changes to the firmware (b).

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Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.baker@microchip.com.*

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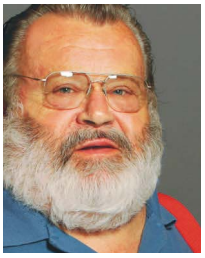

BY RON MANCINI

Anatomy of a voltage-feedback op amp

One of the most common requests I get from engineers is for a comparison of voltage-feedback op amps and current-feedback op amps. It is impossible to determine which one better suits a given application without explaining how each op amp functions. Here, I tackle the voltage-feedback op amp (**Figure 1**).

Precision and CMR (common-mode rejection) are the voltage-feedback op amp's strong points, but its slew rate and frequency performance are subpar compared with those of a current-feedback op amp.

In **Figure 1**, the long-tailed pair, Q_1-Q_2, and the current source, I, form the input stage of the voltage-feedback op amp. Perfect matching of Q_1 and Q_2 causes equal collector currents when the base voltages are equal. Another way to appreciate this matching is to realize that grounding the base of Q_1 effectively puts the base of Q_2 at ground because the voltage drops are equal. The semiconductor process matches the input transistors the best it can. When that matching is inadequate, the manufacturer employs other means of making the transistors appear matched, such as trimming deposited resistors or blowing links.

Connecting IN− to IN+ eliminates the input differential voltage; thus, the input voltage becomes common-mode. Moving the common-mode input voltage up or down 1V does not change the collector currents in Q_1 and Q_2, so the circuit rejects the common-mode voltage. The common-mode-voltage rejection is complete as long as you don't violate the collector- or emitter-current source compliance.

Matching Q_1 and Q_2 ensures that the base-emitter voltages and current gains, β, are equal. An equal base-emitter voltage ensures that no input-offset voltage exists, and equal current gains ensure that the input currents are equal. Equal input currents eliminate the input-offset current, so you can employ external resistors to turn input current into common-mode voltage that the op amp easily rejects. The voltage-feedback op amp's precision stems from its matched input stage.

The voltage-feedback op amp is a voltage-gain device; hence, it has high-impedance nodes, such as those at the collectors of the various transistors. Coupling high-impedance nodes with the slightest stray capacitance causes early frequency roll-off and poor high-frequency performance. Furthermore, the node driving the buffer limits the circuit's slew rate. The prebuffer-stage slew-rate equation is dV/dT=I/C. The output-current source fixes I, and the junction capacitance fixes C, so the internal design of a voltage-feedback op amp limits its slew rate. This type of circuit has limited slew-rate performance unless you can design the circuit to enhance its slew-rate performance. But enhanced slew rate always comes at the costs of increased power and often decreased gain and precision.

In general, the voltage-feedback op amp has excellent precision and CMR coupled with mediocre frequency and slew-rate performance. EDN

Ron Mancini is a staff scientist at Texas Instruments. You can reach him at 1-352-569-9401, rmancini@ti.com.

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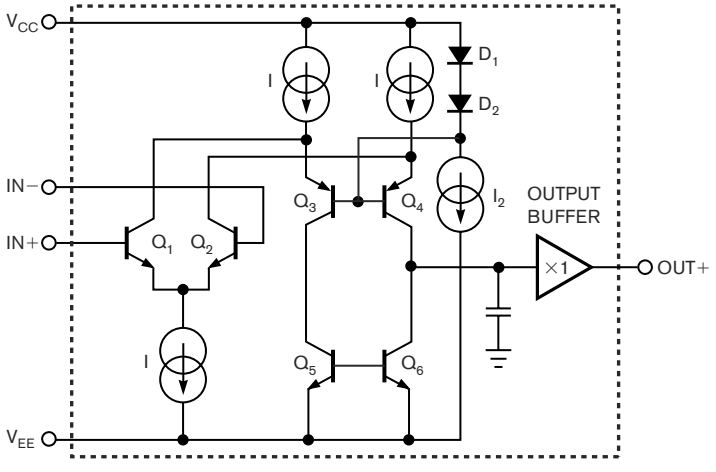

Figure 1 A voltage-feedback op amp uses a long-tailed pair to obtain precision and common-mode rejection.

TEXAS INSTRUMENTS

POWER MANAGEMENT

Analog Applications Journal

BRIEF

Miniature Solutions for Voltage Isolation

By Geoff Jones • *Marketing Manager*

The hot growth in distributed-power architecture has fueled the development of miniature low-power (<2-W) DC/DC converters. As their name implies, these devices minimize the impact of the converter onboard space. They provide point-of-use isolated power conversion for analog circuitry in industrial applications and safety-critical applications such as telecommunications and medical equipment. Additionally, miniature DC/DC converters benefit designers who need galvanically isolated output power or noise reduction in analog circuitry.

In most modern noise-sensitive circuitry, system designers often have a small number of components that require total isolation from their input power supply. It is necessary to isolate the load and noise presented to the local power-supply rails from the main-supply rails of the entire system. Mixed-signal integrated circuit (IC) design, for example, frequently leads to nonfunctional devices because of noise problems. Large amounts of digital noise combined with sensitive analog circuitry often results in interference noise.[1]

Miniature DC/DC converters with galvanic isolation offer very low output noise and high accuracy. Galvanic isolation helps to reduce system noise by providing a floating ground on the secondary side of the converter.[2] The input-to-output isolation can then be used to provide a simple, isolated-output power source; or, it could be used to generate different voltage rails, dual-polarity rails, and/or nonstandard voltages. Also, as a noise reduction technique in analog circuitry, the isolation barrier prevents noise from the digital ground bus from affecting the sensitive analog circuits.

The standard brick-type converter is not well suited for this requirement. In addition to its higher cost, the brick's output power is overkill for applications requiring <2 W. What's more, the installed size of a brick is often prohibitive. Designers require miniaturization to save valuable board real estate. Because they are significantly smaller than even the new sixteenth-brick format (0.29 in^2 vs. 1.17 in^2), miniature DC/DC converters are particularly suited to generating onboard voltages in space-constrained designs.

So why not "roll your own" DC/DC power supply? Discrete component onboard converter designs are a low-cost alternative to bricks and off-the-shelf miniature DC/DC converters. However, fewer designers are developing discrete designs because of their disadvantages. Extra functionality, such as device protection and module-to-module synchronization, are difficult to implement; reliability is often poor; and achieving a small-sized power supply is difficult. In addition, many designers of higher-level products—of which the DC/DC converters are only one component—lack the time to become expert enough in converter design to build their own devices. As a result of these challenges, more and more designers are specifying miniature DC/DC converters for their applications. The converters offer significantly lower risk, much faster time to market, and development-cost savings.

Besides their advantages over bricks and discrete designs, miniature DC/DC converters also provide a compact-sized power solution for point-of-load (POL) power conversion. POL converters enable designers to overcome the challenges caused by the high peak-current demands and low-noise margins of the latest high-performance semiconductor devices. The converters can be placed close to their loads. This minimizes losses caused by voltage drops, helps overcome noise sensitivity and EMI emission issues, and ensures tight regulation under dynamic load conditions.

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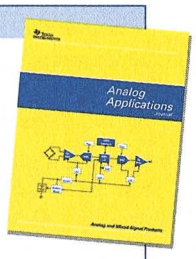

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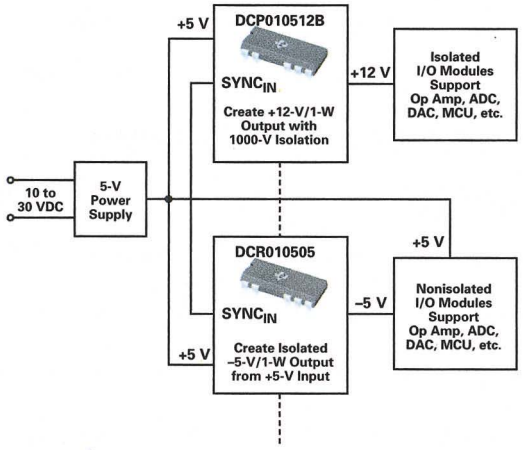
What's available?

Miniature DC/DC converters offered by C&D Technologies, Texas Instruments, Wall Industries, and others benefit designers who require isolation and output current in the 20- to 500-mA range. The converters are available with 5-, 12-, 15-, or 24-V inputs. Single-output converters are available with voltages from 3.3 to 24 VDC. Dual-output converters with voltages from ±3.3 to ±24 VDC are also available. Miniature DC/DC converters offer regulated or unregulated outputs with input-to-output isolation ratings of 1000, 1500, or 3000 VDC. Operating temperature extends from –40°C to +100°C. Due to their high switching frequencies (up to 400 MHz), the converters deliver efficiencies of up to 85%.

Built-in features

For system designers seeking to implement miniature DC/DC converters, the devices offer various built-in features that ease system integration and simplify design. Many of the available products incorporate thermal and short-circuit protection and internal filtering. Some of the more advanced converters allow device-to-device synchronization. If an application uses more than one converter on a PC board, beat frequencies and other electrical interference can be generated. DCP010512B and DCR010505 converters (Figure 1) overcome this problem with a built-in synchronization control that allows multiple converters to be synchronized to one another. The feature makes it easy for designers to synchronize up to eight devices by connecting the $SYNC_{IN}$ pins together. This eliminates electrical interference caused by variations in switching frequencies.

Figure 1. Self-synchronizing DC/DC converters in distributed-power application

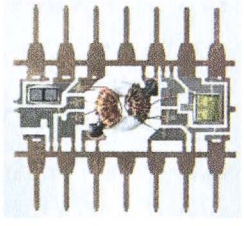


Construction

Today's DC/DC converter technologies continue to focus on higher densities and efficiencies as well as on smaller packages. One of the more innovative converters is manufactured with the same technology as standard IC packages, including dual-in-line (DIL) and small-outline (SO) styles (Figure 2). They use an IC lead-frame as the medium to interconnect silicon devices and magnetic components within the IC package (Figure 3). The result is an isolated DC/DC converter that provides high reliability, excellent thermal management, small size, and compatibility with standard board-assembly processes. The standard IC format also allows tape-and-reel assembly, which helps reduce manufacturing costs.

Figure 2. Miniature isolated DC/DC converter in standard IC package

Figure 3. IC lead-frame



Different configurations

The galvanic isolation of the output from a miniature DC/DC converter allows nonstandard voltage rails to be generated by connecting multiple converters in series. This is accomplished by simply connecting the positive output of one converter to the negative output of another. This configuration allows a wide variety of voltage variations to be produced. The outputs on some dual-output converters can also be connected in series to provide two times the magnitude of output voltage. Figure 4 shows a dual ±15-V converter connected to provide a 30-V rail.[3] Multiple converters connected in parallel often provide a suitable solution for cases where a single converter is unable to deliver the required output power. When parallel connection is used, it is always a good design practice to use parallel converters of the same type. Figure 5 shows two converters connected in parallel.[2]

Figure 4. Connecting dual-output converters in series

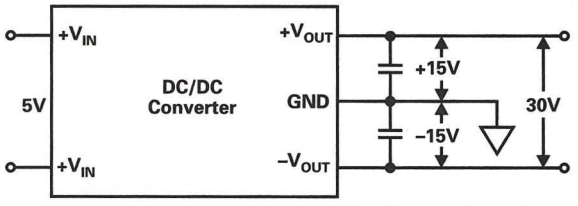
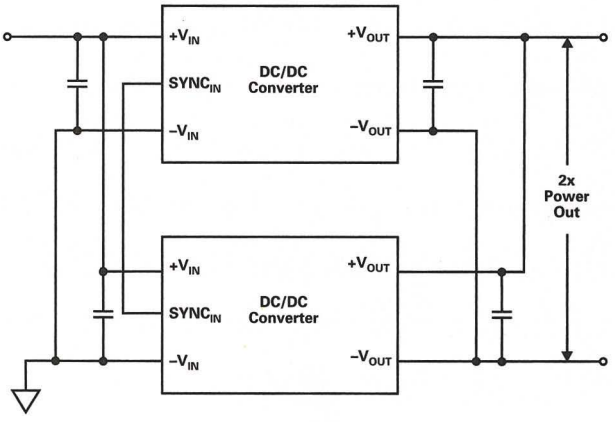


Figure 5. Connecting multiple DC/DC converters in parallel



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Document Title

1. "Noise Reduction is Crucial to Mixed-Signal ASIC Design Success," Electronic Design (October 30, 2000).
2. "Packaged DC-DC Converters Solve Distributed Power Dilemmas," Electronic Design (June 12, 2000).
3. "Miniature, 2W Isolated Unregulated DC/DC Converters," DCP02 Series Datasheet (sbvs011)

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Network delivery

Windows-driven low-power PC-like design delivers video over the Internet, but content will gate success.

Akimbo is the first true consumer product that delivers a PVR (personal-video-recorder)-like experience, albeit with content through a broadband Internet connection (see "Video over the Internet: Services and devices move closer to living-room convenience," *EDN*, Sept 1, 2005, pg 35). The product performed well, but the choice of content may limit its success. This Prying Eyes focuses on what makes Akimbo go. Surprisingly, the design relies on off-the-shelf components and Windows rather than an SOC (system on chip) and low-cost embedded software.

You would think that an SOC for video decoding would lie at the heart of the Akimbo PVR. Such a chip would generally offer better performance in power per watt and potentially lower cost than a processor and chip set from the PC market. But Akimbo based its design on a 733-MHz Celeron processor and the Intel 815 core-logic chip with an embedded graphics controller. A standard PC-centric DIMM provides 64 Mbytes of memory.

Cooling is obviously a key issue in the living-room-centric Akimbo design. Moreover, consumers don't like noisy fans in their living rooms. So, Akimbo relies primarily on large heat sinks on the Celeron processor, the graphics chip, and the Focus FS453 video-scan converter that drives the TV output. A small fan on the side of the main pc board moves air laterally through the box and across the board and heat sinks. But no fans are on the chips, as they are in PCs.

The Akimbo user interface offers no clue that Windows lurks underneath. You might expect that the device would use some royalty-free operating system, because price is a key factor in the success of a product such as Akimbo, and Microsoft isn't license-friendly. But the Akimbo carries a small "powered by Windows XP" label, and Microsoft's Web site states that the design can run either Windows CE 5.0 or Windows XP Embedded. According to Microsoft, the user interface relies on Direct Draw, and the video display relies on Direct Show. The device transmits and stores video in the MPEG-4 format with Microsoft's DRM (digital-rights-management) system, which restricts viewing of the content to only the Akimbo to which it's delivered.

Other ICs in the Akimbo design include the ITE Tech IT8712 Super I/O, the Winbond 39V040 4-Mbyte flash, the ICS 9248 clock synthesizer, the Realtek RTL8101L Fast Ethernet, the Realtek ALC850 audio codec, and the Intel 82801 I/O-controller chips. The ITE chip integrates a host of functions, such as a floppy-disk controller and parallel port, that the Akimbo design lacks. But the chip also includes an infrared remote-control interface, so that's likely why it is present. The remainder of the chips match the Akimbo feature set. Despite its PC legacy, the power needs of the Akimbo design pale in comparison to those of state-of-the-art PCs. Akimbo relies on an open-frame supply with 5 and 12V outputs. **EDN**

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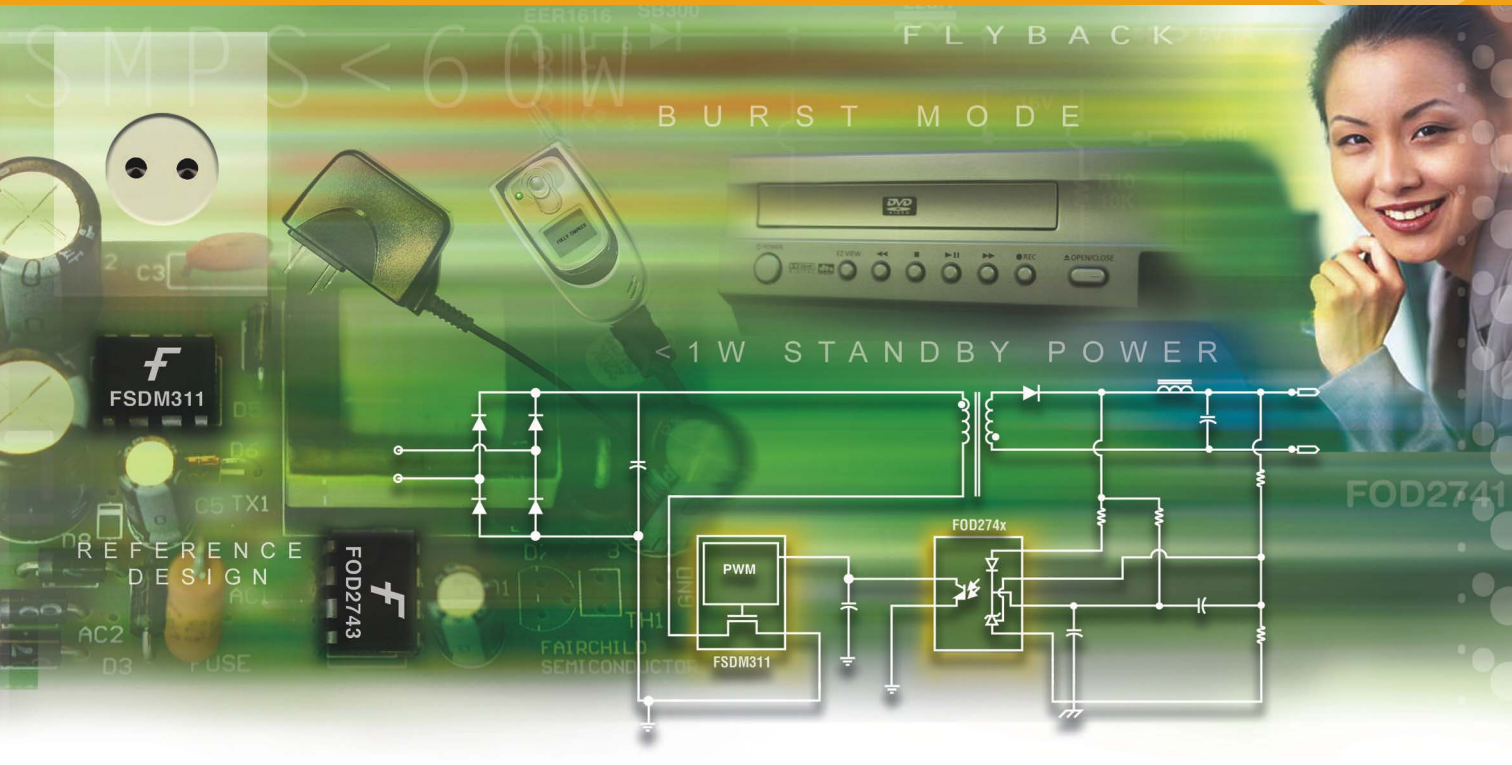

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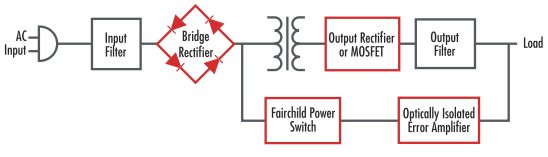

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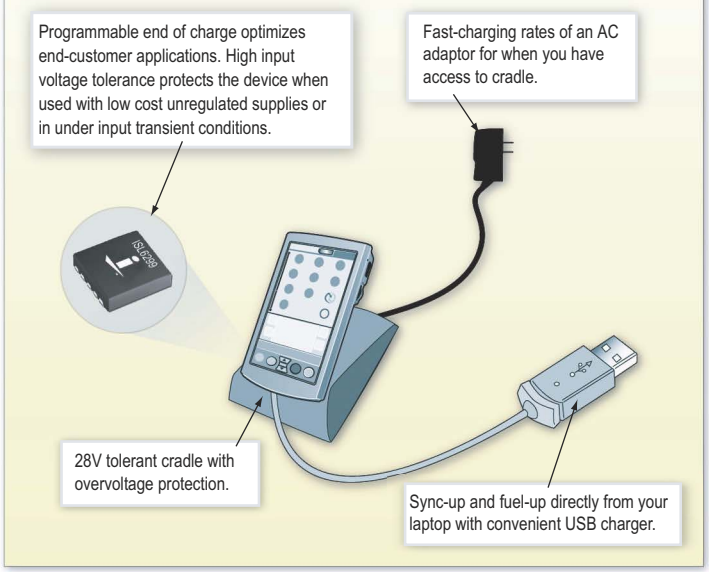

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ENERGY HARVESTERS extract power from light, vibrations

HARVESTING AMBIENT ENERGY FROM LIGHT OR VIBRATIONAL SOURCES CAN FREE POWER-MISERLY DESIGNS FROM TRADITIONAL POWER LINES AND BATTERIES.

Many systems, such as tiny wireless-networked sensor nodes and low-cost calculators for the consumer market, have severely constrained power sources resulting from remote location, cost considerations, portability requirements, or other factors. In addition, the move toward wireless communications, which obsoletes many system cables, makes designers want to further untether systems from power cords and recharge units using energy harvesters. These small devices convert the freely available energy inherent in most operating environments into conditioned electrical power. The most common energy harvesters are based on small solar cells or electromagnetic devices that convert mechanical vibrations.

Energy harvesters also find use in environments that have ready access to power lines, such as factory floors. Roy Freeland, chief executive officer of energy-harvester vendor Perpetuum, points out that initial installation can be a significant portion of system costs for networked machinery monitors. "The cost of taking that factory power and wiring it up to the sensor and transmitter accounts for about 80% of the cost of installing condition-monitoring equipment." In contrast, the installation of self-contained power units with magnetic holders involves only walking up to a machine and snapping the unit in place.

Batteries also can free a system from a power cord but at the cost of limiting the system's service-free life. After two years of usage, a vibrational energy harvester is a superior source to a lithium battery (**Figure 1**, **Reference 1**). If your application's lifetime is 10 years or longer, a vibrational or a solar source is superior to any battery technology. Labor costs can add a prohibitive premium to the system's lifetime-ownership cost, so just changing the battery is not an option.

On the downside, systems relying on harvested energy must operate on a bare minimum of power. Wolfgang Heller, PhD, product-line manager for wireless-sensor manufacturer EnOcean, cautions against trying to design a wireless-sensor network separately from the power source. "We've had discussions with customers who have their own radio and want to buy just the energy harvester. It always turns out that the radio they have consumes 100 or 1000 times more energy per bit transmitted than our design. It's

AT A GLANCE

- Tiny solar panels are the most common energy harvesters.
- Piezoelectric and thermal-gradient technologies will become more common in the next year.
- Only systems with ultralow-power appetites can survive on harvested energy.

not feasible to use these tiny energy harvesters with any other radio."

EnOcean offers network nodes that can receive power from several types of energy harvesters, including light-switch actuators, linear-motion converters, mechanical vibration, thermal gradients, and the sun. EnOcean's PTM 200 light-switch actuator integrates a relay with a magnet and a coil, so that moving the switch to turn the light on or off changes the flux through the coil, generating a voltage (**Figure 2**). The switch module wirelessly transmits the on/off command to the room light. This information is useful in a smart building (**Reference 2**). It also can drastically reduce the wiring labor costs for a building. When the room lights are all under a local wireless network, installing them does not require an electrician. Thermal-gradient-powered devices are candidates for industrial applications in which the production processes produce heat. Thermal-powered harvesters should become commercially available within six months.

OFF THE GRID

EnOcean also makes solar-powered STM100 network nodes (**Figure 3**). The modules have a two-section solar cell; one section is larger than the other. The smaller section charges a small capacitor that powers the sensor and RF circuitry during quick-start/wake-up mode. The larger section charges an ultracapacitor that powers the system during periods of darkness. Says Heller, "If we had only one solar-cell section, it would take hours to start up because the ultracapacitor needs more time to achieve the necessary voltage level. So, we power the quick-start mode with the smaller part of the solar cell, and then we achieve several days of operation in darkness."

EnOcean's solar-powered modules use a polycrystalline solar cell. Polycrystalline cells convert solar energy to electric power at an efficiency of 11 to 16% and are familiar sights on residential and industrial off-the-grid solar-panel systems. Another popular type of solar cell is amorphous silicon, but its efficiency is only 8%, or about half that of polycrystalline. Besides being less efficient, amorphous-

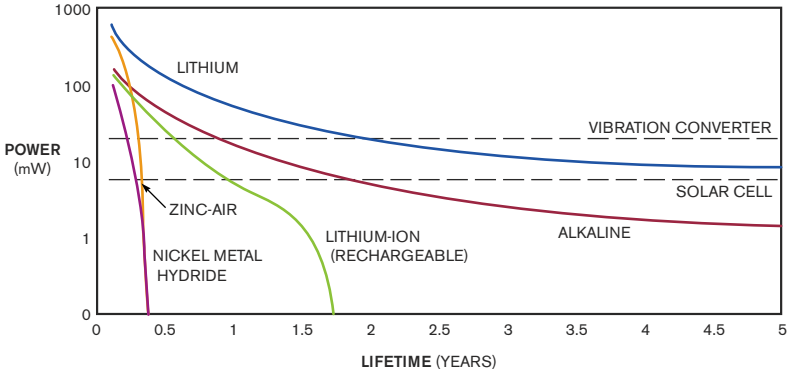

Figure 1 Although lithium batteries can supply small amounts of current for years, a solar-cell or mechanical-vibration energy harvester has a virtually unlimited lifetime.

SOLAR-POWERED CALCULATORS OFFER GUIDELINES FOR LOW-POWER DESIGN

Solar-powered calculators have been available for more than 30 years, and they serve as excellent design examples for ultralow-power portable devices operating on harvested energy. Russ Rosenquist, senior designer for calculator products at Texas Instruments, offers these design tips for power-constrained, processor-based systems:

- **Use a processor with very long instruction words. "The name of the game is to do as much work as possible in every clock cycle. Using very long instructions with parallel paths gets more work done in a clock cycle."**
- **Use process technology with very low leakage, so that each clock cycle draws the minimum energy.**
- **"Extend the clock gating within the processor: When an instruction is not using part of the chip, turn off local clocking signals, so that nodes in that part of the chip don't toggle unnecessarily."**
- **Choose the right architecture for math-intensive systems. Calculations can be in pure binary form with a hexadecimal basis or in BCD (binary-coded decimal). BCD is more efficient in computing cycles and, thus, power.**
- **Use both the rising and the falling edges of the clock cycle. "Today's design tools stress that you use synchronous-design techniques, which implies that you use only one edge of the clock: the rising edge. But, with calculator design, if you can do any work on the falling edge, you do it." Focus on minimizing the number of cycles it takes to complete the calculation. "When you do that, you operate the processor at a lower frequency and still get the answer in a reasonable amount of time."**

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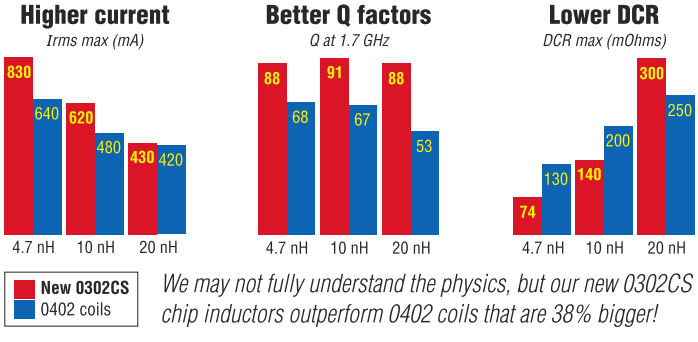

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silicon cells' conversion efficiency degrades 15 to 35% per year in direct sunlight. Despite these significant drawbacks, amorphous cells are popular because they cost about an order of magnitude less than polycrystalline cells—a significant advantage in high-volume consumer electronics. For example, a typical 55×11-mm polycrystalline cell costs about $3 compared with less than 25 cents for an amorphous-silicon cell. One solar-powered electronic device that uses amorphous-silicon cells is the ubiquitous solar-powered calculator, such as that from Texas Instruments.

Russ Rosenquist, senior designer for calculator products at Texas Instruments, breaks solar-cell selection into how much power a system requires based on its computational power and display needs and what size solar cell will generate that power in the expected operating environment. Two typical environments for calculator use are classrooms, which usually have fluorescent lighting, and hotel rooms, which usually have dimmable, incandescent lighting. "We try to design to operate at the lowest light levels you can possibly find in the workplace or school," says Rosenquist. "There is a limit: There are places where people can see the display of the calculator, but there's not enough energy with that light level to actually run the product. We normally design down to light levels of 50 to 75 lux. At that level, you can see pretty well; it's not so dark that you can't see things across the room. That's the lowest level we've been able to achieve with the amorphous panel at a size that's appropriate for our calculator footprint." Another benchmark for what to expect in a well-lit environment is that most school classrooms in the United States have lighting levels of 200 to 500 lux. "Classrooms are well-lit environments," he says.

In addition to the lower cost, one of the advantages of an amorphous-silicon cell is that it's more efficient than a polycrystalline cell under fluorescent and incandescent lighting. Amorphous-silicon cells respond differently to different wavelengths, says Rosenquist. "You get more power out of 50 lux of incandescent than 50 lux of fluorescent—roughly 25% more," he says.

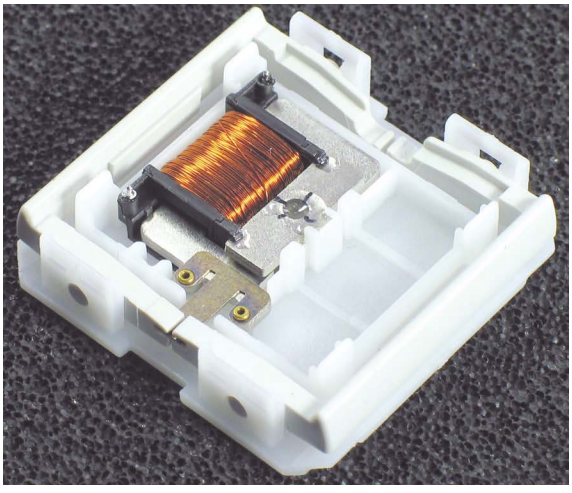


Figure 2 EnOcean's batteryless, 40×40×11.2-mm PTM 200 switch module harvests enough energy to power remote control of light switches within buildings. The actuating force is 5N over 1.5 mm.

Rosenquist also notes that users can sometimes employ a calculator in bright sunshine. In typical room lighting, the solar cell generates less than 1.5V, and in bright sunshine, it may generate much more than 2V. "We put an LED in parallel with the cell, so that, when you're in very bright light, the LED starts to sink a lot of the extra current and hold that voltage at 1.5V," he says. The LED becomes a simple, inexpensive voltage clamp.

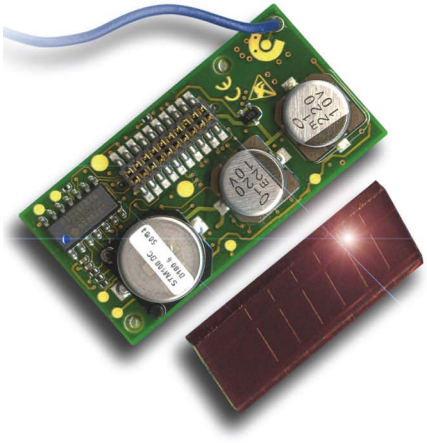


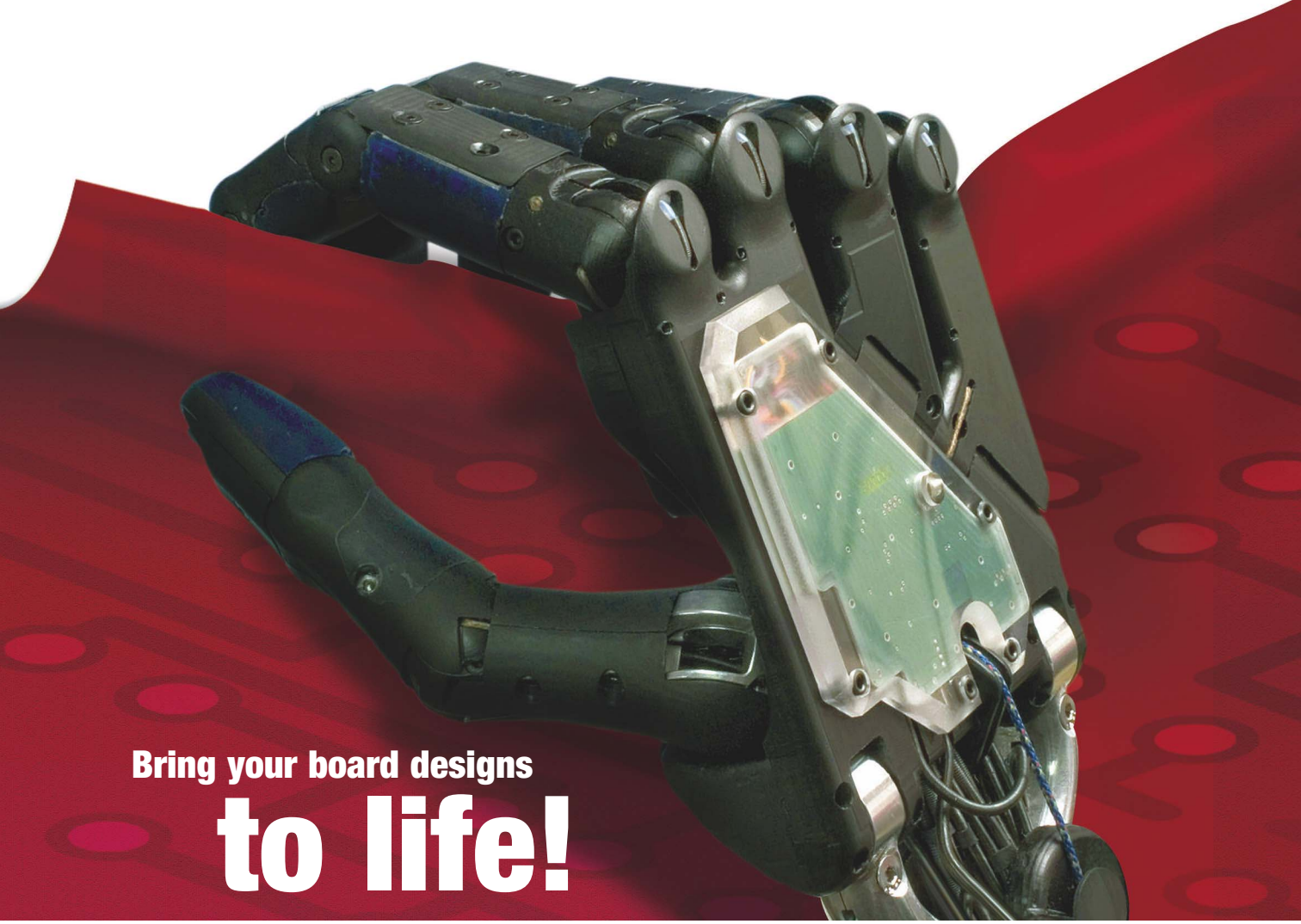
Figure 3 The solar cell that powers EnOcean's STM100 network-transmitter node has two sections: The square area on the left charges a conventional capacitor, and the larger area on the right charges an ultracapacitor.

As with most of the design engineers working with harvested-energy sources, designing your overall system to be miserly with power is just as important as selecting an energy source (see **sidebar** "Solar-powered calculators offer guidelines for low-power design"). (For more on ultralow-power-system design, see **Reference 3**.)

GOOD VIBRATIONS

Not all operating environments have reliable, constant light. For example, machinery-monitoring sensors may not have reliable light but have plentiful vibrational energy. Vibrational-energy harvesters can be either electromechanical or piezoelectric; electromechanical harvesters are more common. Perpetuum's Freeland says the company originally pursued piezoelectric technology but eventually concluded that it simply did not generate enough power at the amplitude and frequency of vibrations in machines and buildings. Instead, Perpetuum turned to electromagnetics, including coils, magnets, and a resonant beam, and designed a generator that could produce significant amounts of electricity from readily available vibrations. "These are vibrations from typical machinery, or even a domestic refrigerator: around 50 Hz in Europe, 60 Hz in the United States, or 100 to 120 Hz. At these frequencies, if you've got 0.5 to 0.1g, then you are generating enough to power electronic circuits." The module includes a power-conditioning circuit that produces 3 or 3.3V dc from the generator's initial ac power. Current depends on the strength of the vibrations but, for typical machinery, can be approximately 1- to 3-mW power generation.

Freeland describes a wireless-sensor sys-



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tem that one of Perpetuum's customers designed. "The device included a temperature and a humidity sensor and transmitted twice a second. Typically, a transmitter needs about 30 mW, but the device transmits for only tens of milliseconds, and there is normally a capacitor in the circuit that is charged up and that then discharges to drive the transmission, which is the heaviest power requirement." Perpetuum's generator costs $30 (volume quantities).

Ferro Solutions also makes vibrational generators. The company based its initial product on electromagnetic technology but has recently patented and produced a piezoelectric version that amplifies the piezoelectric-bender (a strip of flexible, piezoelectric material) magnetostrictive component, which changes shape based on a magnetic field. The price is approximately $30. EDN

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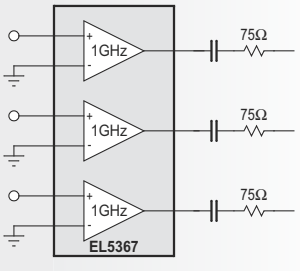

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EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
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EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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Meet Different Needs with NAND and NOR

By ***Richard A. Quinnell***

FOR THE LAST FEW YEARS THE MEDIA has debated which Flash memory technology, NAND or NOR, will emerge as the market winner. This discussion implies that the different Flash technologies are essentially interchangeable in applications, making the two direct competitors for design wins. The reality is, the two technologies address different needs.

Understanding the differences between the technologies begins with their names. The original approach to Flash memory followed the structure of other semiconductor memories, which achieve random access by connecting the memory transistors to the bit lines in parallel. Each transistor has a word line and a bit line connection. In this arrangement, if the word line turns on any memory transistor, the transistor connects drain to source and the corresponding bit line goes low. The logic function is similar to that of a "wired NOR", hence the name NOR for this arrangement.

In 1987, Toshiba proposed the NAND Flash, and its cell structure is arranged as eight memory transistors in series. The transistors are normally on, connecting drain to source through the series and keeping the bit line low. If the word line turns off any memory transistor, the transistor breaks the series connection and the bit line goes high. The logic function is similar to that of a NAND gate.

THE TWO MAIN FLASH MEMORY TECHNOLOGIES, NAND AND NOR, ARE OFTEN VIEWED AS COMPETITORS BUT EACH ADDRESSES A DIFFERENT APPLICATION REQUIREMENT.

These two structures result in differing attributes for the memory devices. The NOR Flash offers fast read access because its memory cells have relatively low resistance. Further, it follows conventional memory architectures, so its behavior in a system mimics that of SRAM, making it easy to design in. File storage and retrieval requires only minimal software, most of which is associated with Flash's need to erase a cell before writing to it.

NOR reads fast, writes slow

The drawback of the NOR arrangement is that writing to cells must be done individually. Writing can take many microseconds each time it is performed. As a result, writing blocks of data to a NOR Flash takes a relatively long time because you cannot program a large number of bits simultaneously.

The NOR Flash also has the disadvantage that its memory cell is larger than that of the NAND Flash. Because each transistor has its own connection to the bit line, the cell requires more metal-layer contacts, making the transistors occupy more die area than in NAND cells, which connect in series in silicon. Because metal-layer connections are the limiting factor in scaling, the NOR Flash always lags NAND Flash in achievable bit density.

The NAND Flash structure allows a page of data to be programmed simultaneously. A page size is typically 2,112 Bytes or 16,896 bits. This greatly speeds write times. On the other hand, the higher resistance of a series connection, compared to the parallel connection used in NOR Flash, means that the NAND bit lines are relatively slow to change state, limiting read access speeds. (See Figure 1.)

But NAND Flash does not offer a conventional memory interface. Controlling a NAND Flash is similar to controlling an I/O device in that device control is achieved by writing to the NAND Flash's internal registers. A command sequence is required in order to perform a read, program, or erase operation. An advantage of this indirect interface is that it enables migration to higher chip densities with no change in pinout.

NAND writes fast, reads slower

Block access also makes NAND Flash unsuitable for truly random access use, such as execution in place (XIP) of program code. If NAND Flash is used for code storage, the system needs to copy the code to RAM in order to execute the code. NOR Flash allows XIP.

A major advantage of NAND Flash, beyond erase and write speed improvements, is that the NAND Flash cell structure uses less die area per bit, This allows a higher bit density for a given fabrication process and a lower cost per bit for NAND Flash as compared to NOR Flash.

These relative advantages and limitations make NAND and NOR Flash architectures suited to different applications. NOR Flash performs better than NAND Flash in code storage applications, where read speed is the most critical parameter. Further, NOR's ability to support XIP means that no additional memory needs to be involved in order to run the stored code. Code storage typically does not require the highest density memory, so the cell size restrictions are not significant in this application.

NAND Flash performs best in data storage applications. It was originally developed to function like and replace magnetic storage, such as disk drives. In data storage, write speed is the most important performance parameter, so the speed advantage of NAND Flash makes it the best architecture for data storage. Read speed is a secondary concern in data storage, although it should be at least as fast as the write speed. The read speed of any Flash memory is greater than its write speed, however, so the performance of NAND Flash meets the read requirements of data storage, as well.

Capacity, however, is a critical concern in data storage. Data storage can require thousands of times the capacity needed for code storage. As a result, both total capacity and cost per bit become important for data storage needs. The smaller cell size of NAND Flash further points to this architecture as the best choice for data storage.

Flash types fit different applications

The differing application strengths for Flash architectures thus allows for both NOR and NAND to co-exist in the market, and even in the same design. In a cell phone, for example, NOR Flash can serve as code storage where the memory's XIP capability eliminates any need for shadow RAM. NAND Flash can serve as data storage for large memory files such as photos and video.

The situation may eventually change, however. NOR Flash is increasing in density and in write speed with each process generation. Although NOR will never catch up to NAND, these density increases allow NOR to stay ahead of increasing storage requirements in smaller applications. For those applications, NOR's design simplicity gives it a cost advantage over NAND Flash.

NAND Flash, on the other hand, continues to lead in cost, density, and write performance. The existence of a powerful NAND Flash controller is making design-in easier, so for larger applications NAND Flash becomes the lower cost option.

ADDITIONAL INFO

- *To learn more about Flash memory visit www.edn.com/NANDflashmemory*
- *For more information on Toshiba's NOR and NAND Flash go to www.toshiba.com*

The largest single market for Flash memory is the cell phone, and high-end cell phones are using ever faster processors. These processors are beginning to force use of shadow RAM for code storage regardless of the Flash in use because no Flash technology is keeping pace with high-end processor read speeds. In addition, high-end cell phones are increasing their need for data storage to provide feature convenience. The addition of cameras, movies, MP3 audio, gaming, and Internet access to phones requires significant amounts of low-cost storage.

These trends are affecting the sweet spot for Flash memory. The high performance applications are beginning to favor NAND Flash for both code and data storage. NOR will still have a home in low-performance code storage, however, so both architectures will continue to co-exist in the market. All that remains uncertain is when the high-volume markets will switch to NAND alone. ■

ABOUT THE EDITOR: *Richard A. Quinnell was an embedded systems designer for 15 years before turning to technology journalism. He was a staff writer for EDN for 10 years and is now a contributing editor and freelance writer for a number of high-tech publications.*

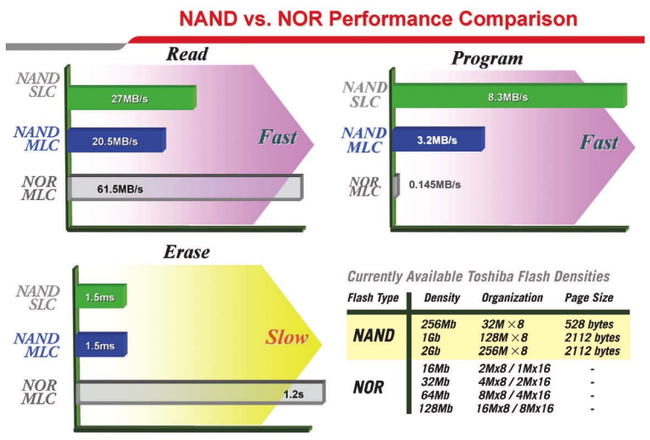

Figure 1. *NAND and NOR Flash architectures have different performance characteristics, with NOR having the edge in read speed while NAND offers faster write and erase.*

SOURCE: TOSHIBA

BY WARREN WEBB • TECHNICAL EDITOR

Embedded-design shortcuts

LOW-COST DEVELOPMENT KITS PROVIDE DESIGN TEAMS WITH READY-MADE TOOLS TO BATTLE GROWING SOFTWARE COMPLEXITY AND SHRINKING PROJECT SCHEDULES.

As customers' performance expectations skyrocket, embedded-system designers must at least consider updating processor and communications technologies for each new project. Yet, the problem with system revisions is the significant learning curve necessary for becoming proficient with a new architecture and associated development tools. It often takes months to uncover all of the nuances and fine details of a new tool set. To address these problems, most board- and silicon-level vendors offer low-cost evaluation or development kits that quickly demonstrate product performance and ease the transition to new hardware and software.

The contents of a design-support or -evaluation kit vary depending on the featured product and the marketing approach the vendor adopts. Hardware ranges from a simple peripheral module that you can plug into your design to a stand-alone embedded system with processor, memory, peripherals, programmer, and breadboarding area to test your application circuitry. Some vendors simply provide a reference design that may or may not be available as a physical product. Software offerings include drivers for unique silicon all the way up to a complete development environment for processor products. Some vendors assume that you have access to a compiler or provide limited trial versions. Many processor and single-board-computer vendors include configured, open-source software, such as the Linux operating system, to jump-start the development process.

HANDS-ON PROJECT

AT A GLANCE

- Developers are tempted to upgrade processors and their related tool sets on each new project to benefit from faster, lower cost silicon.
- Silicon and board vendors use development kits to attract new customers and steer existing customers to their next generation of products.
- A common graphical integrated development environment allows designers to move to new tools with a shortened learning curve.
- Designers may need to replace low-cost evaluation boards with higher cost development tools to gain full access to all product features.
- With remote access and dedicated development hardware, designers can evaluate products and develop software using their Internet browsers.

Development kits are major marketing vehicles for many vendors to capture new customers and steer existing customers to the next generation of in-house products. Michael O'Donnell, a marketing manager in Freescale's Developer Technology Organization, says, "Freescale delivers 40,000 to 50,000 evaluation or demonstration boards and reference designs annually to make it easier for our customers to step into our silicon. There's a fairly common set of tools around those boards available directly from Freescale using the CodeWarrior brand of tools or from our third-party ecosystem. There are increasing performance requirements in the marketplace that result in dramatically more complex silicon designs. Our goal is to make those complex designs easy for customers to adapt to, and that is the reason for focusing on reference designs and evaluation platforms that have a common layer of software, or application-programming interface, across all of our architecture families."

COMMON INTERFACE

To reduce the learning curve, several vendors provide work-alike products with a common IDE (integrated development environment). IDEs provide instant access to a compiler, an assembler, a project-source-code manager, an editor, a debugger, a simulator, libraries, and other development accessories. The Eclipse project is an example of an open-source IDE that several major technology vendors, universities, and research institutions support. Eclipse provides the interface to a range of tools for software development, including modeling, language development, testing, and performance evaluation (**Figure 1**). Similarly, Microchip Technology provides users a proprietary MPlab IDE that works with all of the vendor's PIC-micro processors. You can download the IDE without charge from the Microchip Web site. The most common equipment setup for product assessment and development is to load the IDE software onto a desktop host PC with some type of communications channel to a prototype or an evaluation board containing the target processor. You use the communications channel to download object code and control execution of the target for debugging or monitoring performance. Before the target hardware becomes available, developers can use a software-processor simulator running on the host or a general-purpose evaluation board in place of the target prototype.

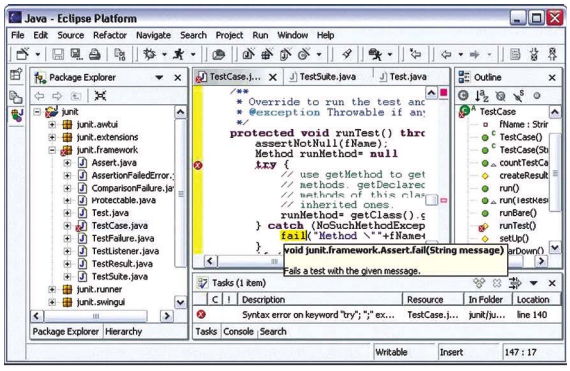

Figure 1 The open-source Eclipse integrated workbench gives tool designers a common user interface, such as this Java-program-development tool.

As system complexity increases, programmers prefer a higher level language, such as C, to gain portability and take advantage of off-the-shelf function libraries and drivers. C compilers should conform to ANSI/ISO standards to ensure portable code. Much of the power of a high-level language such as C comes from the built-in and extendable library functions. Basic library functions include I/O, memory management, and math routines. When a programmer creates a particularly useful function, he can save it in a library and reuse it on subsequent projects. Operating systems, networking stacks, and other third-party-software elements usually are available in library form. Most small-system C compilers are cross compilers, which means that the compiler runs on the host machine and produces object code for another machine.

To survey the ease of installation and operation of development and evaluation kits currently available for embedded-system designers, *EDN* selected several products for appraisal in our lab. The first was the C6713 DSK (DSP starter kit) from Spectrum Digital, a stand-alone development platform that enables users to evaluate and develop applications for the Texas Instruments C67xx DSP family. The DSK also serves as a hardware reference design for the TMS320C6713 DSP.

The DSK comes with power-supply cabling software and a multipurpose evaluation board for the processing needs of audio, industrial, and medical applications. In addition to the TMS320C6713 DSP operating at 225 MHz, the board includes an AIC23 stereo codec, 16 Mbytes of synchronous DRAM, 512 kbytes of flash memory, and user-accessible LEDs and DIP switches. The DSK works with TI's Code Composer Studio development environment and includes

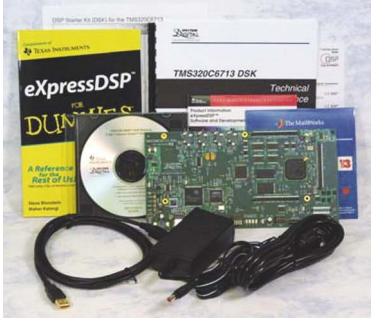

Figure 2 The Spectrum Digital C6713 DSP starter kit allows users to evaluate and develop applications for the Texas Instruments C67xx DSP family.

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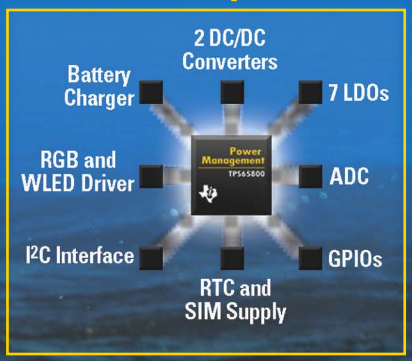

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a version tailored to work with the board. Although the software installation, hardware setup, and initial operation took less than 30 minutes, the sample LED-blinking tutorial was elementary and provided little insight into the performance of the DSK (**Figure 2**). The TMS320-C6713 DSK is available online from both Texas Instruments and Spectrum Digital for about $400.

VISUAL DEVELOPMENT

In a similar vein, the ADSP-BF537 EZ-kit Lite from Analog Devices provides developers with a low-cost method for evaluating a popular Blackfin processor and system peripherals, including the IEEE 802.3 10/100 Ethernet MAC (media-access controller) and CAN (controller-area-network) 2.0B controller. The kit includes a processor-evaluation board along with an evaluation version of the VisualDSP++ development and debugging environment that includes a C/C++ compiler, assembler, and linker (**Figure 3**). The kit also contains sample application programs, a power supply, cables, and a pair of stereo headphones. The software installation went without problems, and the development environment was able to recognize the evaluation board after configuration and license registration. The EZ-kit includes a simple LED-blinking example, along with more in-depth software to exercise the audio, Ethernet, and CAN interfaces. The VisualDSP++ development environment makes it easy to edit, compile, and link application programs and then load, run, and set breakpoints for debugging. The ADSP-BF537 EZ-kit Lite costs $350 and is available from the Analog Devices Web site. Both the Blackfin and the Texas Instruments evaluation-board devices provide for third-party plug-in boards to extend the feature set and showcase compatible products.

The cost of evaluation-board hardware and support software makes it difficult for vendors to showcase all of their capabilities and still provide lower priced kits. Roy Druian, marketing manager in the Freescale Networking and Computing Systems Group, explains, "We offer a series of fairly expensive application-development systems that designers use when they roll up their sleeves to develop their systems and end products. We felt that we also needed to produce a much lower cost tool to determine if a product has the required features, functions, and performance without a big investment." According to Druian, Freescale's networking organization has created a series of "quick-start" boards that wrap around the company's major products. These boards typically sell for a few hundred dollars to less than $1000 and come with Linux, so an operating system is available for customers to use, or they can drop in their own. Customers can also download their application code to see whether it works. "We have designed these kits to include everything a designer needs, such as cabling, power supplies, and run control," says Druian. "The customer can buy the product, open the box, and be evaluating the product in less than 30 minutes. Once the customer has done the initial evaluation and it looks like something that he wants to consider further, we would recommend that he move on to the complete application-development system, which would then give full access to all of the capabilities of the product."

Manufacturers also offer evaluation and development boards for peripheral or add-on products. The VR Stamp tool kit from Sensory is one example that provides development support for the company's embedded voice-recognition technology. "The VR Stamp makes it quick and easy for a developer to incorporate voice recognition and speech synthesis as the human interface for embedded products, such as set-top boxes, medical instrumentation, and industrial controls," says Bill Teasley, Sensory's vice president of engineering. Sensory based the VR Stamp module on the company's RSC-4128 voice-recognition system on chip, which includes a 16-bit ADC, a 16-bit DAC, digital filtering, RAM, ROM, output amplification, timers, and comparators. The VR Stamp module's 40-pin-DIP footprint also packs in flash memory, serial EEPROM, main-clock and real-time-clock crystals, and power-noise-management components (**Figure 4**). The VR Stamp tool kit includes a special edition of Sensory's Quick T2SI tool that allows speaker-independent vocabulary-set development using simple text input to create commands. The complete tool kit, including development software, sample programs, a C compiler, two VR Stamps, and a programming board, retails for $495. The VR Stamp modules

Figure 3 The ADSP-BF537 EZ-kit Lite from Analog Devices includes a Blackfin-processor-evaluation board and the VisualDSP++ development environment.

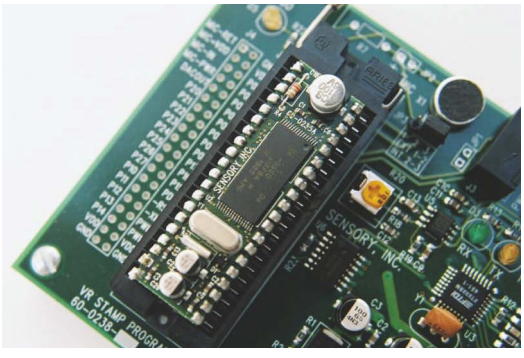

Figure 4 The VR Stamp tool kit from Sensory provides development support for the company's embedded voice-recognition speech-synthesis technology.

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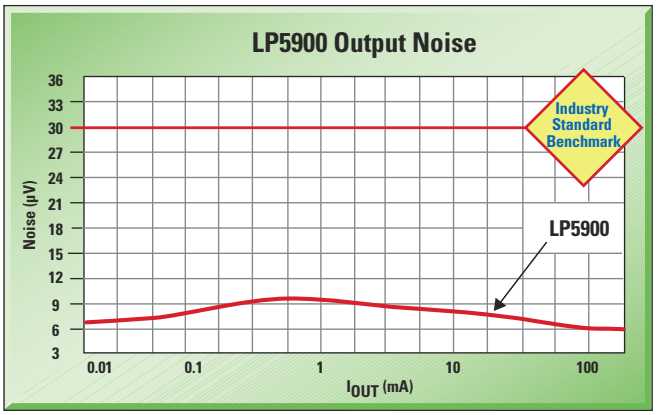

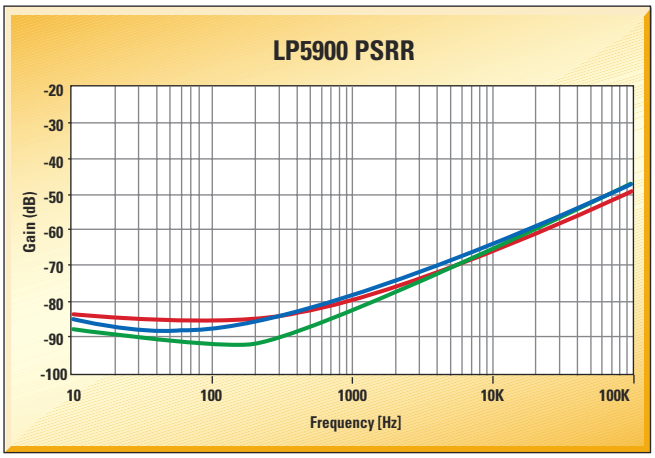

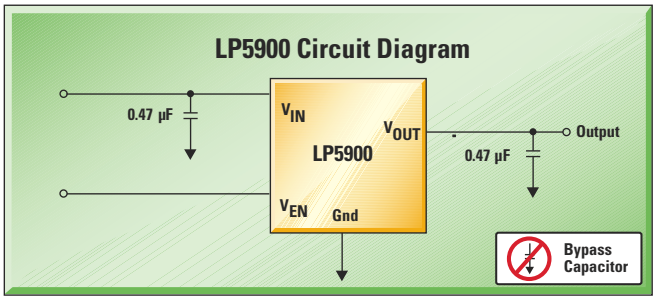

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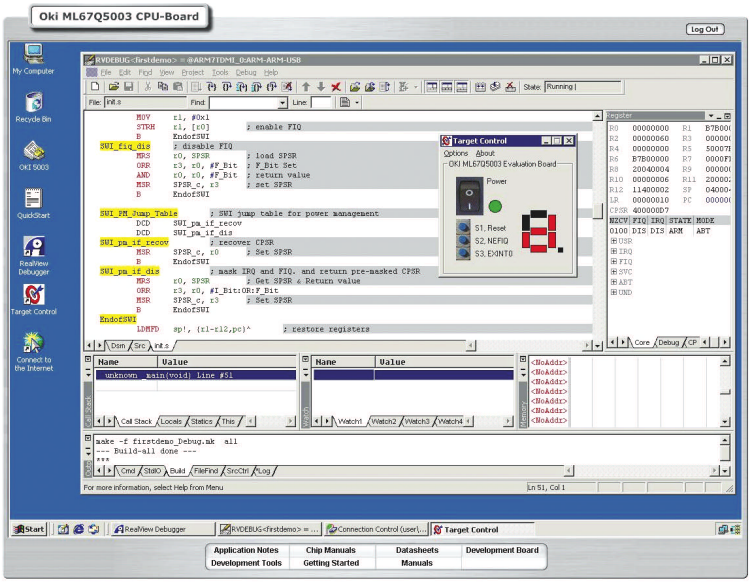

Figure 5 TechOnLine's VirtuaLab gives developers remote online access to several development kits, including the Oki ML67Q5003 CPU board.

sell for less than $30 (volume quantities).

Although the final development-kit hardware and software installation time can be less than an hour, the entire process may take weeks and includes justification of funding, issuing a purchase order, waiting for delivery, unpacking, and locating a suitable PC. To bypass all these steps, TechOnLine's VirtuaLab allows you to immediately evaluate hardware and software tools using only your Web browser. This free service provides documentation and remote access to a selection of tools through a virtual-desktop connection to a PC with hardware attached. A reservation system allows hardware scheduling as much as six months in advance, although we observed instant access in several cases. Each engineer has LDAP (Lightweight Direct Access Protocol)-protected network storage available, as well as a local computer to access, upload, or download files. Between each session, the environment returns to a known, safe state to prevent residual interactions.

With online development tools from vendors such as Altera, Analog Devices, Freescale, Intel, Xilinx, and Renesas Technology, TechOnLine offers a variety of technologies, including 16- and 32-bit processors, DSPs, FPGAs, and network processors. To test the system, we logged onto the Oki ML67Q5003 CPU board, an emulation kit for developing and debugging embedded application programs for ARM-based, 32-bit microcontrollers. This setup allows users to write and execute code on an ARM-based microprocessor and debug with ARM's RealView debugger development kit (**Figure 5**). Users have access to on-chip peripherals, such as an ADC, UART, and I^2C, plus control of a seven-segment LED. The board clocks the processor at 60 MHz and includes 512 kbytes of flash memory and 32 kbytes of RAM. We were able to log on, initialize the board, read the "getting-started" instructions, build the demonstration program, and step through execution in less than an hour.

Development tools and short cuts may shorten the evaluation and learning curve at the beginning of a project; however, no magic tools exist to eliminate the detailed design effort required to fashion a successful embedded product. It still takes long hours and hard work. However, rest assured that tools vendors will continue to deliver support products that optimize the development process and ease the transition from one project to the next. EDN

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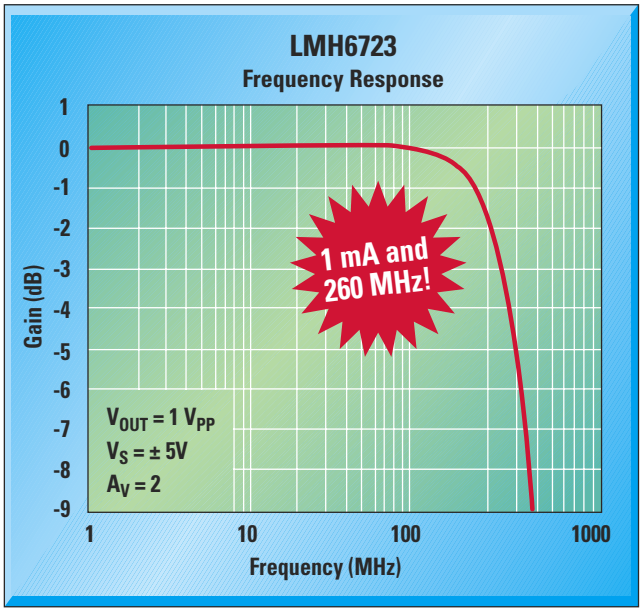

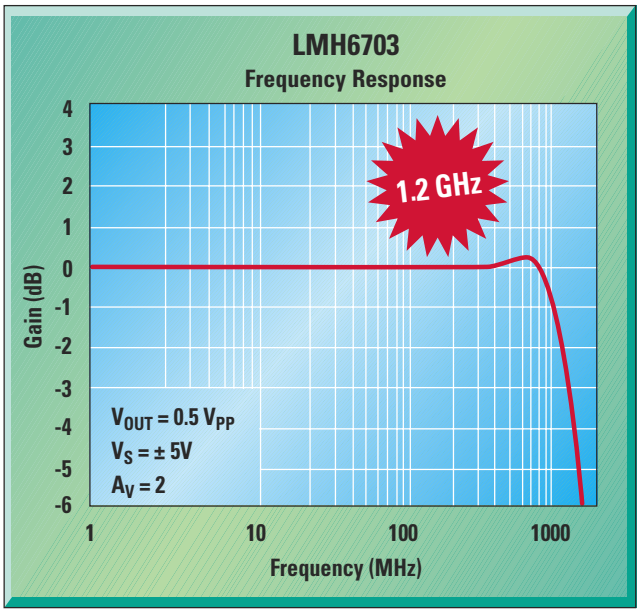

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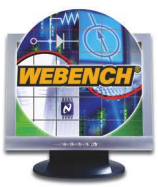
LMH6704	Single, programmable gain (-1, +1, +2), shutdown op amp	650 MHz SSBW, 400 LSBW, 2nd/3rd HD: -62/-78 dB at 10 MHz



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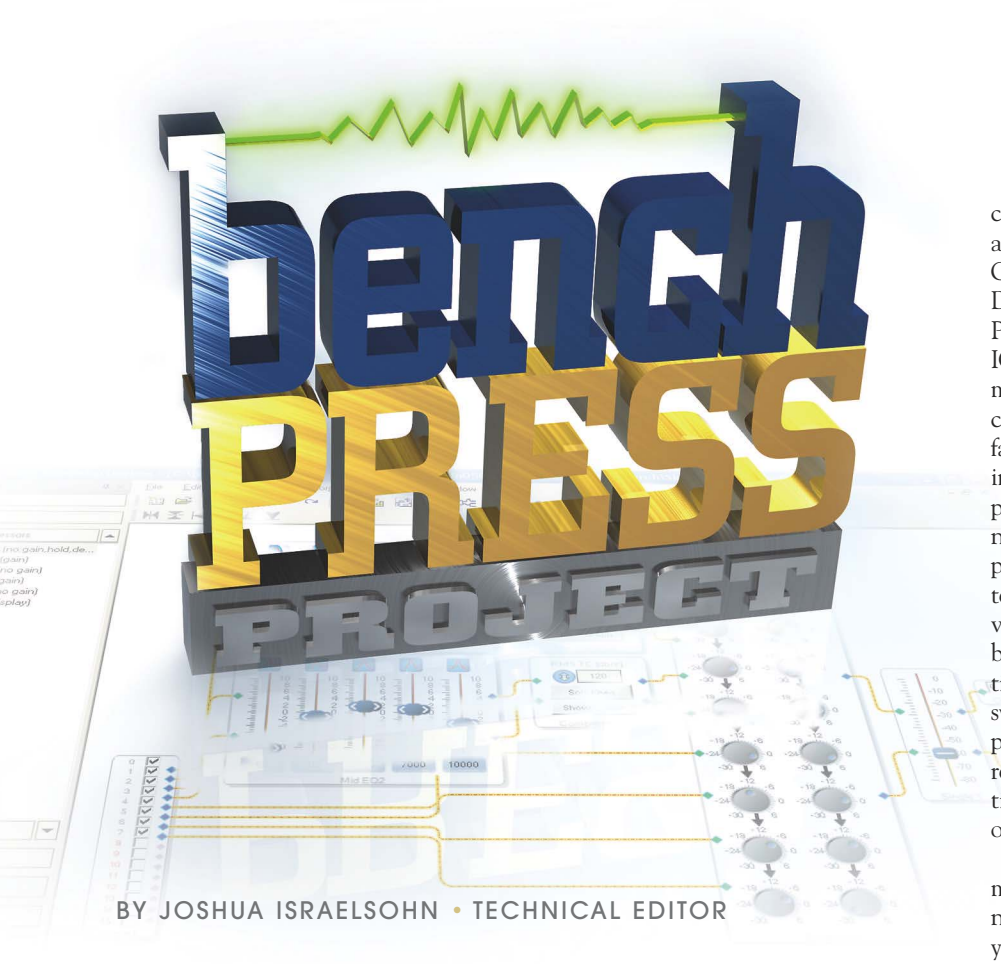

BY JOSHUA ISRAELSOHN • TECHNICAL EDITOR

PART 2

FLEXIBLE SILICON: GUI-programmable audio processors

A TREND IN SIGNAL-PROCESSING ICs OFFERS SIMPLE AND DIRECT PARAMETRIC CONTROL AND FUNCTIONAL PROGRAMMABILITY. TAKING FULL ADVANTAGE OF FLEXIBLE CHIPS, HOWEVER, MAY DEMAND FLEXIBILITY IN YOUR DESIGN METHODS, AS WELL.

Part One of this two-part series introduced the concept of flexible silicon—signal processors that are programmable in environments that express functional and parametric behavior in application-relevant terms (**Reference 1**). Interacting with the signal processor at this elevated level of abstraction frees the OEM designer from many implementation details that regard signal streams in terms of instantaneous voltages or individual digitally encoded samples. Instead, the designer can focus on issues of functional implementation and performance expressed in the same terms as the system-design goals.

To make this distinction more concrete, this study has concentrated on two audio-signal processors—the XS-125-4 Class D power-amplifier module from D2Audio, which was the primary focus in Part One, and the AD1940 SigmaDSP IC from Analog Devices, which is the primary focus of this installment. In both cases, the devices must accommodate the fact that, at their most basic level of implementation, signal processors manipulate audio signals as time-domain phenomena, yet, at the application level, people prefer to consider audio signals in terms of their spectra and signal envelopes. Designers often leave this bridge between the time-domain and application-level models of audio signals to the system's user interface. The fact that the processors bridge the two concepts results in familiar-looking GUI presentations and could simplify implementation of the system interface.

Though the programming environments that accompany these flexible signal processors can greatly speed parts of your design cycle, your design methods may need to exhibit some flexibility, as well, particularly in design verification. Your familiar schematic-capture and simulation tools don't have these devices ready and waiting as drop-in blocks, macros, or behavioral models. Instead, your verification efforts will likely depend to a great extent on direct measurements. But, given the nature of the devices and the means of control they offer, the most meaningful measurements will be those that are in application-relevant terms, as well. Common instrumentation, such as logic analyzers, oscilloscopes, and voltmeters—though helpful for signal tracing—are less helpful for parametric verification in this environment than are more sophisticated signal analyzers. Your verification success, therefore, may critically depend on a solid familiarity with your measurement equipment and your understanding of its limitations (see **sidebar** "Flying on instruments").

FLEXIBLE TO THE CORE

The Analog Devices AD1940 is a flexible, general-purpose, GUI-programmable audio processor that operates ahead of a system's signal-distribution facilities. Bob Adams and his SigmaDSP team

AT A GLANCE

- The ratings:
  - Flexible silicon parts—great!
  - Support hardware and soft ware—mostly terrific.
  - Documentation—not ready for prime time.
- Software interfaces are convincing, if occasionally cumbersome.
- Though the software tools are mostly accurate, be sure to confirm with stimulus and response measurements to prevent unwanted surprises.

developed the family of parts to which the 1940 belongs. To develop those devices, Adams and the team exploited a custom DSP core, which they designed and optimized for audio-signal processing. As a general-purpose audio processor, the 1940 cannot do with a fixed arrangement of processing blocks, as was the case with the XS-125-4. Instead, its GUI programming-and-control environment, SigmaStudio, presents a drawing surface reminiscent of familiar schematic-capture tools, with a library of 61 processing cells in nine categories from which you can choose. Two additional categories provide system resources, such as hierarchal structures and simulation stimuli and probes. They also include signal sources, such as a tone, pink noise, white noise, and beep generators.

The simulation stimuli and probe cells enable real-time interactive spectral simulation. SigmaStudio allows you to develop signal-flow block diagrams offline without attaching the development hardware. The diagram that **Figure 1** depicts, for example, is part of a tutorial exercise I completed after dinner one night at the dining-room table. The next morning, I connected my laptop to the AD1940 evaluation board through a USB port, downloaded the file, and ran test sweeps from the AP SYS-2722 through the system. A comparison of the plots in **figures 2a** and **2b** indicates that the SigmaStudio simulation properly accounts for the equalizers' interband interactions and predicts the system response that the SYS-2722 measures. The straight-line plot falling along the −6-dB line in **Figure 2b** derives from output channels 2 and 3: signals that the equalizers do not process. These curves, which indicate a 0.4-dB rise in the lowest decade and a 0.35-dB drop-off in the top octave, indicate that similar behaviors, which appear on the Channel 0 and Channel 1 outputs, are not due to the equalizers' deviation from their predicted behavior.

The constant 6-dB difference that **figures 2a** and **2b** depict derives from the fact that **Figure 2a**'s plot simulates the equalizer's transfer function—a relative measure—whereas **Figure 2b**'s is an absolute measure of the system's performance with reference to 0 dBFS (decibels full-scale). Though it is reasonable to set an equalizer to provide, say, 6 dB of gain at some frequency, a digital-audio system cannot produce an output of 6 dBFS: Unlike analog systems, digital-audio systems have no linear headroom above full-scale. To prevent the system from clipping, therefore, this measurement requires a stimulus signal from the generator no greater than −6 dBFS. In practical systems, inputs can reach 0 dBFS, so a real implementation of this circuit would need to include volume-control cells to manage the signal amplitude in advance of the equalizer. Analyze your design's gain structure to ensure that you can't clip an internal node. Using an equalizer to boost frequencies complicates the issue, whereas cutting is always safe with respect to clipping hazards. Also note that, unlike observations you might make of signals in the time domain, spectral plots are graceful at the onset of clipping. Raising the input level, say, 2 dB, results in spectra with peaks that appear to have lower Qs than the equalizer's settings indicate, rather than flattop peaks. A test for your system's gain-structure plan would include a THD (total-harmonic-distortion) measurement with a 0-dBFS sweep with spectral shaping cells turned up as far as your application allows. A somewhat more sophisticated approach is to build adaptable structures that exploit the AD1940's dynamics-management cells. Consider the trade-offs when deciding between upstream and downstream sensing.

The measurement of this circuit employed a POF (plastic-optical-fiber) link from the AP SYS-2722's digital generator to the AD1940 evaluation board's Toslink SPDIF input. The analyzer took the device under test's outputs in pairs from 1/8-in. TRS jacks through unbal-

(continued on pg 68)

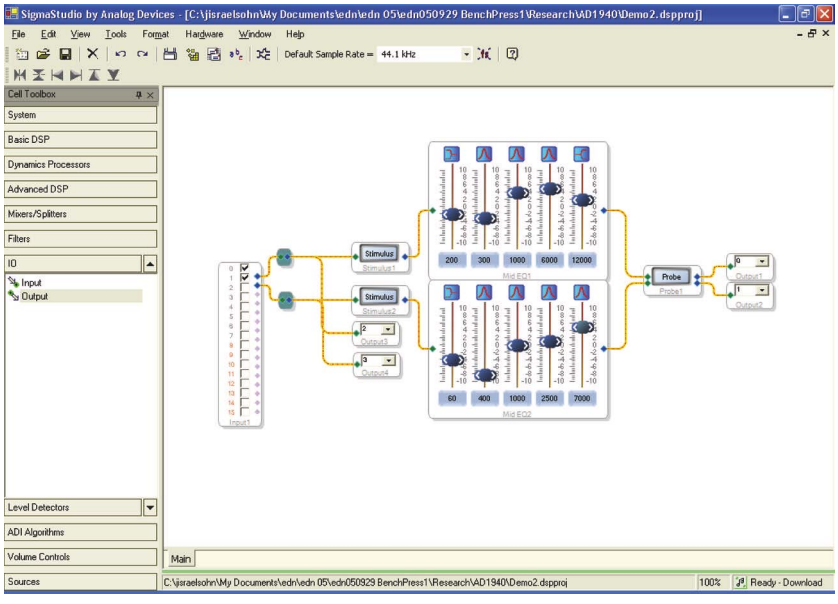

Figure 1 A test design using the AD1940's SigmaStudio design environment allowed rapid confirmation of the processor's parametric equalizer module. In this case, the SYS-2722's dual-domain capability provided a system stimulus in the digital domain and analysis in the analog domain, which simplified switching output-channel pairs.

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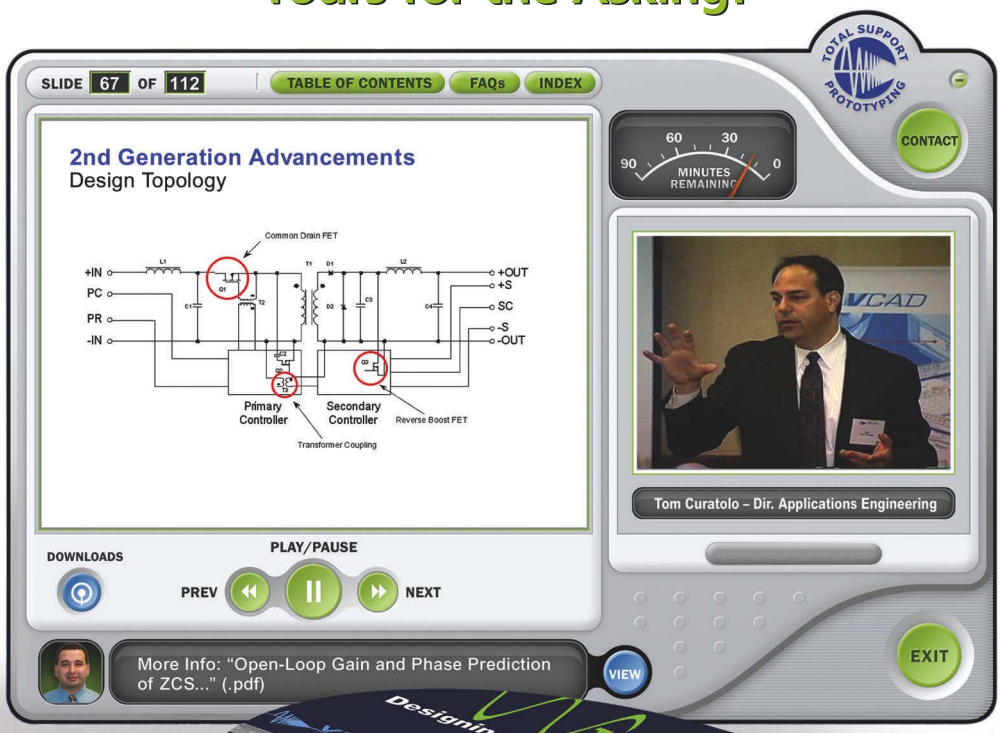

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FLYING ON INSTRUMENTS

My rule for working with test equipment with which I'm unfamiliar is to take sufficient time in advance to learn about the instrument's capabilities, proclivities, operating requirements, and controls. It may sound insultingly simplistic, but the fact remains that anyone can generate data, and many do. Making solid measurements and correctly interpreting the results are more difficult tasks. The first step to distinguishing between the two is understanding the capabilities and limitations of the instrument (Reference A). The better a DUT (device under test) performs, the more difficult it becomes to meaningfully measure its performance and not the residual errors of the test setup and environs.

Audio Precision's AES-17 filter serves as an example: The filter's spectral response can predictably affect test results but do so in a way that an operator lacking familiarity with the measurement system could misinterpret. A plot of the XS-125-4's THD (total harmonic distortion) operating at −0.5 dBFS (decibels full-scale) into an 8Ω load falls precipitously starting at 7 kHz (Figure A). You'll see this plot shape in characterizations of many digital-audio devices with analog outputs, but the shape does not describe the DUT so much as it describes the filter. In the case of the XS-125-4, the third harmonic evidently dominates the THD at full power. At 7 kHz, the dominant distortion residue falls into the AES-17 filter's narrow transition band (Figure B). By 10 kHz, the second harmonic is nearing the end of the filter's passband, and, by 12 kHz, there's little left in the measurement beyond the amplifier's noise floor and a small leakage term representing the analyzer tracking filter's finite notch depth. So, what's the THD doing through the interval from 7 to 20 kHz? This measurement gives us no clue, and discovering the answer in any application in which the harmonics in question approach the Nyquist frequency requires detailed knowledge of how both the DUT and the test environment process artifacts that approach or pass through the Nyquist frequency.

I've on a number of previous occasions worked with Audio Precision analyzers. The most recent interaction, though, was a couple of years ago (Reference B), so this was my first experience with the SYS-2722. The dual-domain instrument can generate and analyze signals in either the analog or the digital domains and, therefore, suits cross-domain analysis in which the instrument provides the test stimulus in one domain and tracks and measures the response in the other domain. This capability came in handy when I was examining the AD1940 and its evaluation board. The generator and analyzer can drive and receive analog signals through balanced XLR or unbalanced BNC connectors. Digital signals appear on balanced AES/EBU, unbalanced SPDIF, or optical Toslink ports. Digital ports operate at all standard audio-sampling rates to 197k samples/sec.

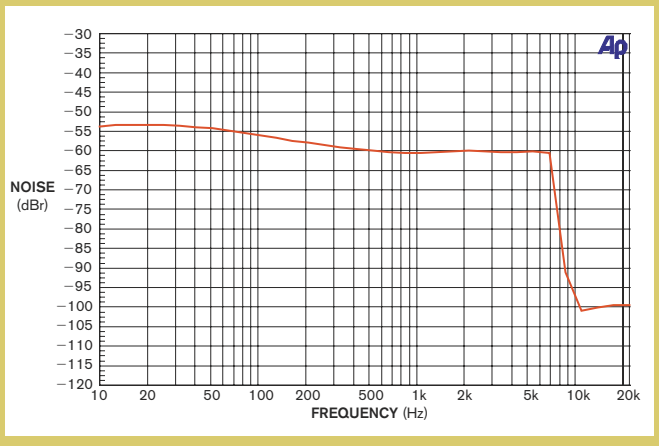

Figure A The XS-125-4's THD+N operating at −0.5 dBFS into an 8Ω load falls precipitously starting at 7 kHz, due to the fact that the third harmonic falls into the AES-17 measurement filter's transition-band response.

The instrument's capabilities are extensive, yet its user interface is well-designed and generally uncluttered. In addition to the instrument's extensive documentation, Audio Precision has produced a five-DVD tutorial course on audio measurements–a valuable accessory for those not steeped in the craft.

In addition to the SYS-2722 analyzer, Audio Precision supplied a DCX-127 multifunction module, which provides precision dc sources, measurement capabilities, and digital I/O. The company also supplied an SWR-2122U unbalanced switcher, which is a handy device for managing multichannel measurements, for example. The accessories connect to the SYS-2722 through the AP control-bus interface, as does the host PC.

I spent a good deal of time with the AP SYS-2722 and accessories before I could find anything to criticize. It's a solidly built system apparently designed by people who use the equipment, so the instrument is almost immediately comfortable to operate. Of the few annoyances I did collide with, all have easy work-arounds.

If you connect accessories such as the DCX-127 to a SYS-2722, the multifunction module must be powered; otherwise, it apparently drags down the control bus. Upon launching the control software, you will get an error message informing you that the analyzer is either improperly installed or is

itself unpowered. Technically, this message is true: You could say that an unpowered DCX-127 is an improper element of the installation. Still, the message struck me as a bit vague, considering the nature of the–admittedly operator-induced–fault that I finally located. If the documentation mentions the need to power all devices on the control bus, I missed that part. In the end, I powered both the SYS-2722 and the DCX-127 from the same outlet strip and used the strip's switch to control power to the test equipment.

The control-bus cable that connects the analyzer to your PC is a bit short and constrains the relative placement of the two pieces of equipment. According to the company's application-support group, however, you can add a DB-25 extension cable to the instrument end of the cable. As long as the cable is of reasonably high quality, you should be able to extend the tether another meter or so.

I used a laptop PC with the analyzer, so the control-bus cable terminates to a single-slot PCMCIA card. The PCMCIA connector is the most fragile part of the system. My experience with similar connectors from the bad old days of PCMCIA dial-up modems is that they reliably fail before any other part of the systems with which they are associated. Although I understand that the weakness derives from the PCMCIA standard's mechanical specifications, other industries have developed more robust connection methods. For example, manufacturers of PCMCIA cards for modems, Ethernet, and FireWire ports have long since developed card extensions that flare out to fairly large and beefy plastic enclosures for more robust connectors. Such a modification to the AP PCMCIA card would remedy that card's weakness. In the meantime, if you use a laptop with a SYS-2722, be careful about where you situate the computer and how you dress the interface cable.

Last, though you may fix plot colors for the screen presentation or allow them to rotate through a color cycle, graphs you export use colors from the color cycle whether you like it or not. This is not just a matter of taste: A yellow graph on white paper is simply unreadable, and coercing the system to cycle to another color has proved to be something of a challenge that the operator shouldn't need to take on. According to Audio Precision, a simple cure is to export the graphs as WMF (Windows-meta-format) files and bring them up in a graphics program that allows you to manipulate vector images. Ungroup the plots and change the color and line weight of each one in turn to yield an appearance best suited to your purposes. We tried that approach at *EDN* with mixed results, using Adobe Illustrator as the graphics program for the manipulations. We ended up publishing plots that I exported from the analyzer in TIF format.

Given the extensive capabilities the SYS-2722 brings to the bench, these few points seem minor. They can derail you for a time, and a loss of bench time could be costly if you don't commit a reasonable interval to familiarizing yourself with the equipment you intend to use. Once you master it, though, the SYS-2722 sets a performance, handling, and documentation standard to which other instruments might aspire.

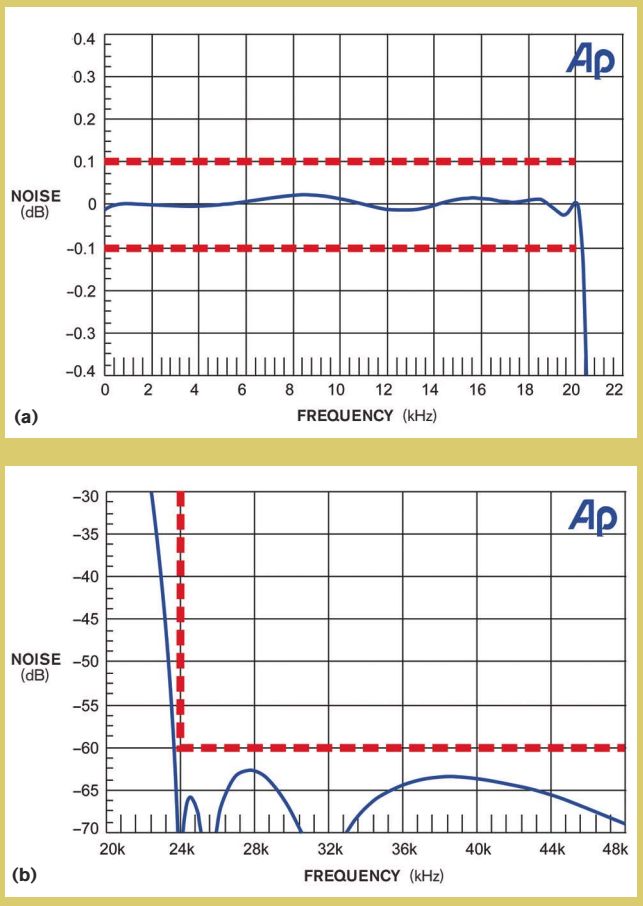

Figure B Audio Precision's optional AES-17 filter provides a flat passband with low ripple (a) and better than the −60-dB spec-required stopband attenuation (b) without adding more than 4-ppm THD in the 20-kHz passband. The red lines correspond to the AES-17-1998 spec limits.

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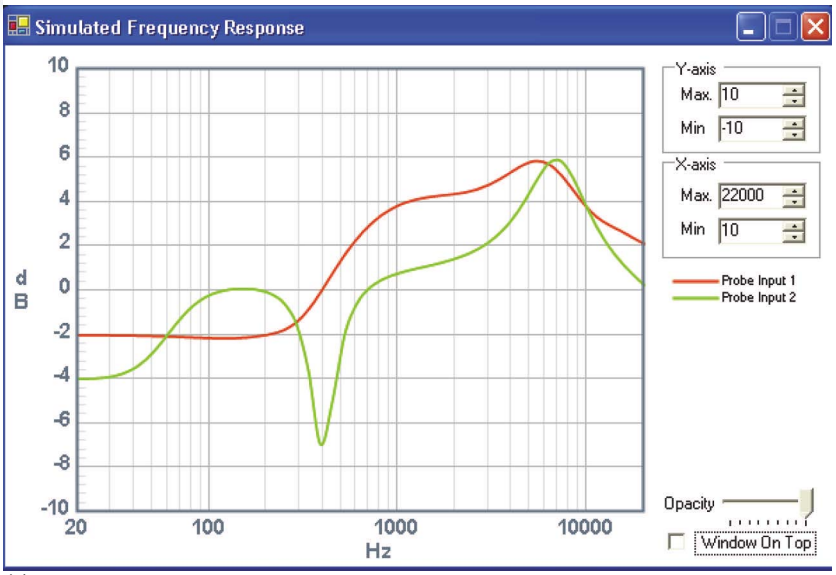
A Williams, Jim, "The taming of the slew," *EDN*, Sept 25, 2003, pg 57, www.edn.com/article/CA323017.

B Israelsohn, Joshua, "Pour your own programmable analog," *EDN*, June 12, 2003, pg 38, www.edn.com/article/CA302236.



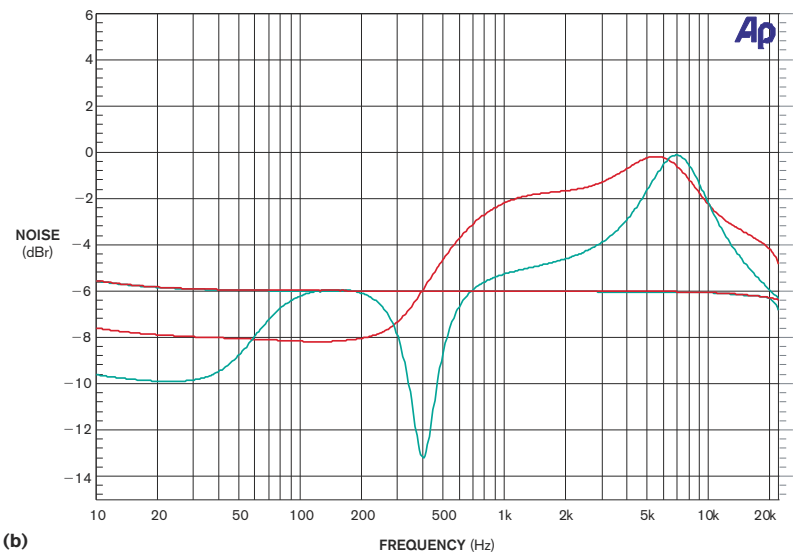


Figure 2 The SigmaStudio simulation (a) properly accounts for the equalizers' inter-band interactions and predicts the system response that the SYS-2722 measures (b). The straight-line plot falling along the −6-dB line in (b) derives from output channels 2 and 3, signals that the equalizers do not process. The constant 6-dB difference between (a) and (b) is due to the fact that (a)'s plot is a simulation of the equalizer's transfer function—a relative measure—whereas (b)'s is an absolute measure of the system's performance with reference to 0 dBFS.

anced, shielded leads. The AD1940's signal I/O resides strictly in the digital domain. An AD1939 codec provides the evaluation board's analog-I/O facilities; the codec adds greatly to the evaluation board's versatility. Less apparent, however, is the I/O flexibility inherent in the AD1940. The audio processor can receive or transmit audio data in two-channel I²S, left- or right-justified formats, or eight- or 16-channel TDM (time-division-multiplexed) streams.

The AD1940 evaluation hardware and SigmaStudio software form a seamless, reasonably responsive operating environment with a mostly well-behaved user interface. However, precisely setting virtual rotary controls is more difficult than

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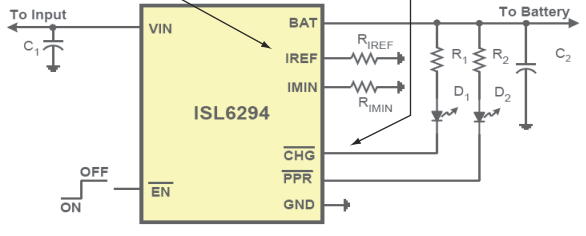
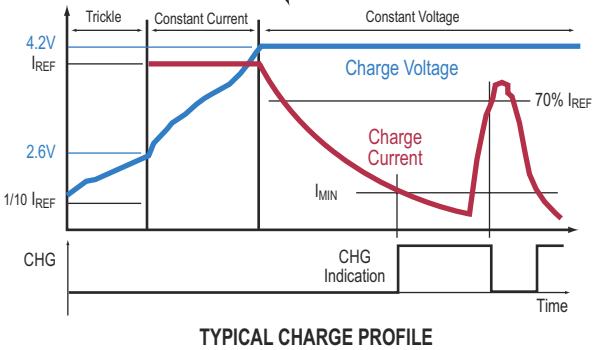
The constant current I_{REF} is set with the external resistor R_{IREF}. The constant voltage is fixed at 4.2V.

End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



TYPICAL CHARGE PROFILE

Key Features:

- 2mm x 3mm 8 Ld DFN package
- 28V maximum input voltage
- Programmable end-of-charge current with status interfaced to a micro device through CHG pin
- Thermaguard™ charge current thermal foldback for thermal protection
- No external blocking diode required
- Integrated pass element and current sensor
- 1% voltage accuracy
- Trickle charge for fully discharged batteries
- Less than 1µA leakage current off the battery when no input power attached or charger disabled
- Input over-voltage protection
- End-of-charge indication with large hysteresis to prevent unwanted re-charge

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similar controls on other platforms. The wiring paths are not user-adjustable, and symmetrical-cell arrangements can often result in overlapping paths, which, though mostly harmless, are difficult to read and can slow visual verification that the design agrees with the designer's intent. Barring any change in the SigmaStudio software, you can mitigate this effect by imposing spatial offsets between cells in your project work space.

The current SigmaStudio documentation is not up to the quality of the software itself. The library documentation's table of contents, for example, omits some items that are actually documented, though the search facility can usually find those items in short order if you know how to search for them. Explanations of many cells avoid many of the less obvious cell features. Although you can generally ignore this documentary weakness when using cells that implement familiar functions, it can slow down your project development when you need to invoke a less familiar function. The hardware documentation is likewise overly terse and lacks both a map and a narrative explanation of the board's layout and features. The SigmaDSP team is evidently aware of the need for better documentation and is working to soon upgrade it. EDN


You can reach Technical Editor Joshua Israelsohn at jisraelsohn@edn.com.

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- Flexible signal processors also exist that operate in the analog domain. For more information, go to www.edn.com/article/CA302236.
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REFERENCE

1 Israelsohn, Joshua, "Flexible silicon: GUI-programmable audio processors: Part One," *EDN*, Sept 29, 2005, pg 60, www.edn.com/article/CA6258590.

ACKNOWLEDGMENTS

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Monolithic Dual Output DC/DC Converters

High Performance Analog Solutions from Linear Technology

Multioutput DC/DC Converter

The LTC®3548 is a dual output, high efficiency, 2.25MHz, synchronous buck regulator that delivers up to 800mA of continuous output current from one channel and up to 400mA from the other. Using a constant frequency and current mode architecture, the LTC3548 operates from an input voltage range of 2.5V to 5.5V, making it ideal for single cell Li-Ion, multicell alkaline or NiMH applications. It can generate two independent output voltages as low as 0.6V, enabling it to power the latest generation of low voltage DSPs and microcontrollers.

Figure 2 shows an application schematic of the LTC3548. Its 2.25MHz switching frequency allows the use of tiny, low cost ceramic capacitors and inductors less than 1mm profile. The LTC3548 uses internal switches with an $R_{DS(ON)}$ of only 0.35Ω to deliver efficiencies as high as 95%. It also utilizes low dropout 100% duty cycle operation to allow output voltages up to V_{IN}, further extending battery run-time. No load quiescent current is only 40µA (both channels) and <1µA in shutdown, ensuring optimal battery life.

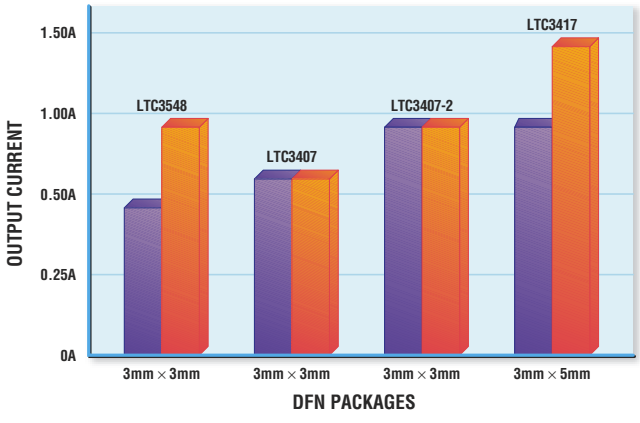


Figure 1. Dual Monolithic Synchronous Buck Converter Family

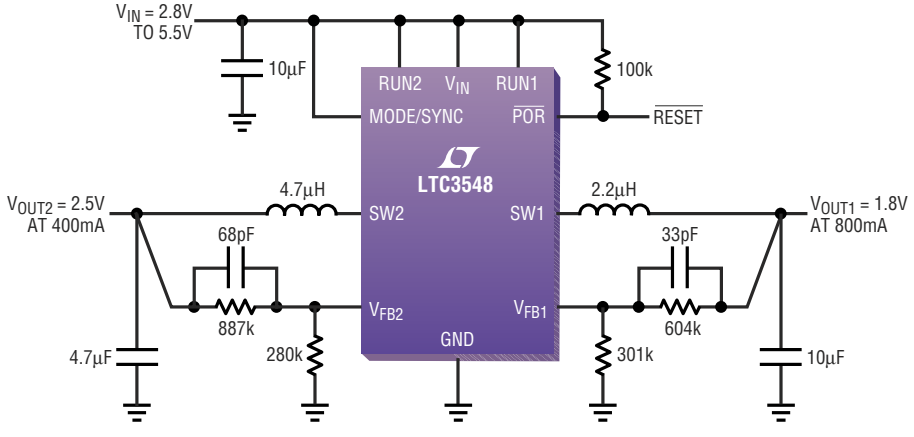


Figure 2. Dual Output Supplies from 5V with LTC3548

Monolithic Dual Output DC/DC Converters

The LTC3548 utilizes automatic Burst Mode® operation to reduce gate charge losses when the load current drops below the level required for continuous operation, providing optimum efficiency at light loads. If the application is noise sensitive, the user can disable Burst Mode, replacing it with a lower noise pulse-skipping mode. The LTC3548 also offers power-on/reset outputs. Thus, if either output falls outside of ±8.5% regulation (after a 175ms delay for output voltage "settling"), the LTC3548 provides a POR Low, telling the system that one or both of the outputs are out of regulation, allowing the main processor to reset the system if necessary. Other features include short-circuit protection and optional external synchronization capability. Furthermore, the LTC3548 is stable with ceramic capacitors, achieving very low output voltage ripple.

The dual architecture, tiny externals and a 3mm × 3mm DFN (or MSOP-10E) package combine to make the LTC3548 the most compact synchronous step-down solution available for dual output voltage rails. The LTC3548 is ideal for handheld applications that require dual outputs of up to 800mA and 400mA, high efficiency and very small solution footprint.

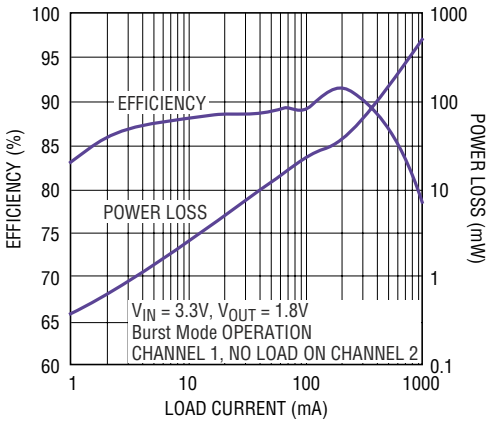
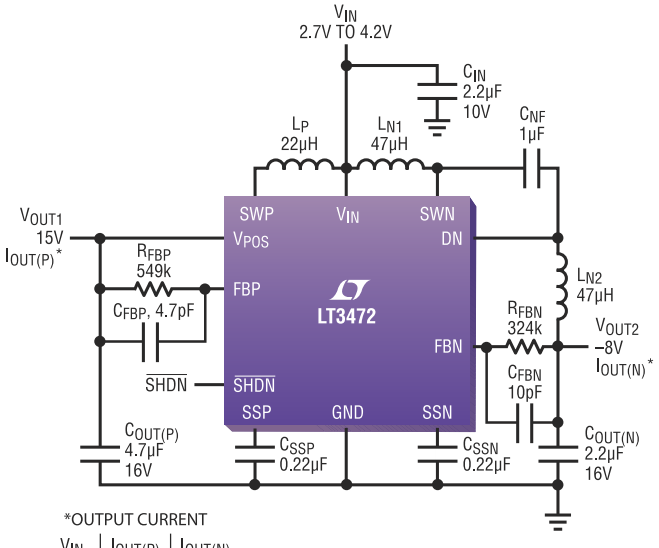


Figure 3. LTC3548 Efficiency and Power Loss vs Output Current

Single Converter Provides Positive and Negative Supplies

Charge coupled device (CCD) imagers, LCDs, op amps and many other circuits require both a positive and negative power supply. Typically, two DC/DC converters are used—one for the positive supply and another for the negative supply. However, the use of two ICs and their related circuitry add cost and complexity. There are single converter topologies that develop plus/minus supplies, but usually the second output suffers from poor regulation. In addition, in order to produce a second output of different amplitude, non-standard, transformer turns ratios or post regulators become necessary, which also increases cost, complexity and efficiency losses.

The LT®3472 dual DC/DC converter simplifies the design of dual, positive and negative, supplies by combining two switchers that have



*OUTPUT CURRENT

V_{IN}	$I_{OUT(P)}$	$I_{OUT(N)}$
4.2V	45mA	65mA
3.3V	35mA	50mA
2.7V	25mA	35mA

Figure 4. LT3472 Schematic for Li-Ion Input Delivering Positive and Negative Outputs

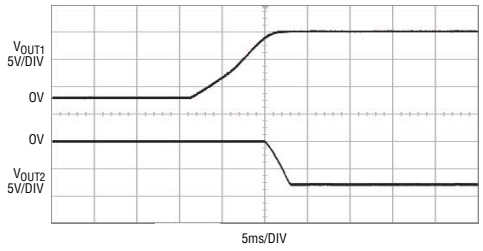


Figure 5. LT3472 Start Up Sequence

independent control loops and ±34V output ranges. Figure 4 shows a circuit using the LT3472 that produces two independently regulated power supplies from a single Lithium-Ion cell: a 15V, 25mA supply and a –8V, 35mA supply. A typical application for this would be for amplifier circuits that need to output a true 0V with only a single positive supply available. A low current negative supply and boosted positive supply rail permit full amplifier output swing from 0V to $V_{BATTERY}$.

The Schottky rectifying diodes are integrated into the LT3472 which shrinks and simplifies the solution. Each supply requires only one resistor to set its output voltage. The LT3472 works well with input voltages as high as 16V. Also, it includes an output sequencing feature that allows the negative supply to ramp up only after the positive one has reached 88% of its final value, providing a controlled turn on as demonstrated in Figure 5. In situations where inrush current is a problem, the LT3472 offers a capacitor-programmable soft start feature that allows the designer to individually program the ramp rate of each output. This feature allows the designer to reduce inrush current to any arbitrary level. Figure 6 shows the supply efficiency.

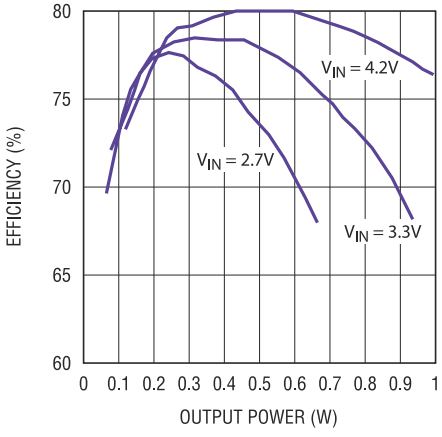


Figure 6. LT3472 Efficiency for Both Outputs Loaded at 10% Increments

600mA Ultralow Noise Synchronous Converter

High efficiency, low ripple current and a small footprint are critical power supply design requirements for cell phones, MP3 players and other battery-powered portable devices. The LTC3448 delivers excellent performance in each of these areas. It is a high efficiency monolithic, synchronous buck regulator using a constant frequency, current mode architecture (see Figure 7). It achieves very low output ripple by automatically shifting to linear regulator operation at load currents below 3mA and pulse skipping operation at moderate load currents. This is a critical feature in applications such as cell phones, where low power supply noise is required while in standby mode. The combination of a 1.5MHz or 2.25MHz switching frequency and a tiny 3mm x

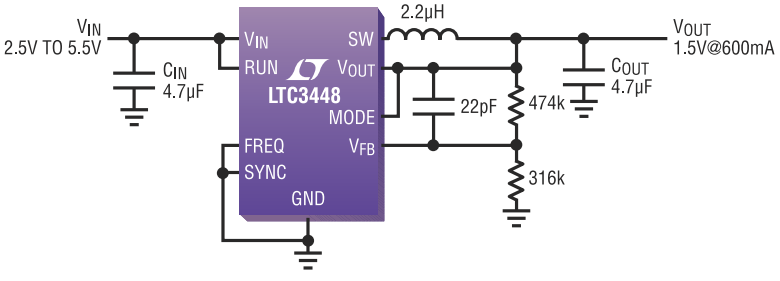


Figure 7. LTC3448 Schematic for Li-Ion to 1.5V at 600mA

Monolithic Dual Output DC/DC Converters

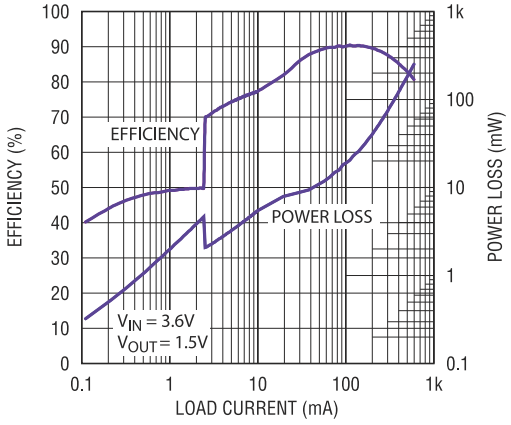


Figure 8. LTC3448 Efficiency and Power Loss vs Output Current

3mm DFN package (or MSOP-8) provides a solution footprint of less the 0.12 square inches.

The LTC3448 automatically shifts gears to maintain high efficiency and low noise over a wide range of load currents. For normal loads, it operates as a current mode constant frequency converter which yields well-defined ripple frequencies. At load currents below 3mA, it automatically shifts to linear regulator operation to maintain <5mV$_{P-P}$ noise and reduce the quiescent supply current to 32µA.

No external sense resistor is required to detect the load current. Simply tie the MODE pin to V_{OUT}. The LTC3448 uses a patent pending technique to monitor the behavior of the switching regulator to determine the load current and to enter linear regulator operation when appropriate. The crossover between switcher mode and linear regulator mode can also be controlled externally by driving the MODE pin high or low.

The LTC3448 has a 2.5V to 5.5V input voltage range, perfect for single cell Li-Ion battery-powered applications and is available with an adjustable output voltage. Its 100% duty cycle provides low dropout operation, extending battery life in battery-powered handheld devices. Low output voltages are easily supported with the 0.6V feedback reference voltage. Switching frequency is selectable to either 1.5MHz, or 2.25MHz. Alternatively it can be synchronized to an external clock applied to the SYNC pin. This high switching frequency operation allows the use of small surface mount inductors and capacitors. The LTC3448 also saves space with an internal synchronous switch, eliminating the need for an external Schottky diode. Efficiencies of 90% are attained in single cell Li-Ion powered applications at 200mA.

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BY BARRY CALDWELL • VITESSE

Board decoupling using a standard methodology

TO DEAL WITH THE SIDE EFFECTS OF INCREASED CLOCK SPEEDS AND FREQUENCIES, ENGINEERS MUST BYPASS DI/DT TRANSITIONS AND REDUCE NOISE.

As Moore's Law has marched through the 1990s into the new millennium, each process node has brought a doubling of density with increased clock and data-transfer speeds and frequencies. Each node, however, also includes the nasty side effects of faster chip, board, and system di/dt transition-voltage noises, as well as signal jitter. To deal with these side effects, engineers need to know how to correctly bypass and decouple high-speed di/dt transitions to reduce noise that the system contains or radiates in some form of EMI.

To achieve this goal, it is important to devise a method of addressing the issues involved in picking and placing bypass and decoupling capacitors for high-speed digital chips, boards, and systems.

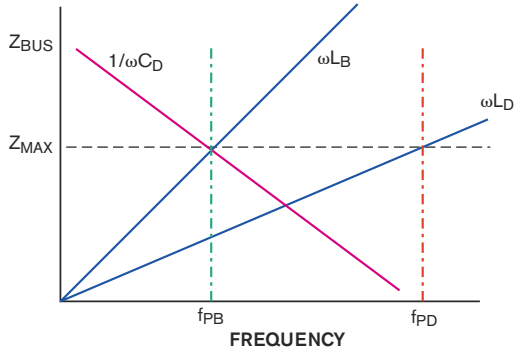


Figure 1 At point f_{PB}, impedance starts switching to inductive impedance; at point f_{PD}, inductance triggers a chain reaction leading to unacceptable amounts of voltage noise.

FINDING THE NOISE SOURCE

The purpose of decoupling a digital chip or board is to remove unwanted frequency noise from the system at any level. To accomplish this task, you must first look at the source or cause of the unwanted noise. In almost all instances, di/dt or ΔI noise is the source. For a digital chip or system, a change in the digital state of the chip or system from either a logic-zero state or a logic-one state brings about a current surge that causes a current-level change. Knowing di/dt or ΔI can help you find the amount of decoupling that a chip needs and then determine the system or board-level decoupling, but you first need to develop a method for finding ΔI:

$$I_{PER\ GATE} = \frac{V}{R_{TTL}} \text{ or } C\frac{dV}{dt_{CMOS}}. \quad (1)$$

TABLE 1 CHIP, DRIVER, AND I/O-RING-DECOUPLING PARAMETERS

Chip, bus, or both			ΔI per pin	Δt	ΔV_{NOISE} (mV)	Data-sheet per-pin capacitance
40-MHz oscillator, 3.3V			2 mA	1 nsec	50	15 pF
PCI-X microprocessor, eight drivers	I/O 3.3V	46[1] power/ground pairs	24 mA	0.8 nsec	50	12 pF
PCI-X microprocessor, 96 drivers	PCI-X I/O 3.3V	46[1] power/ground pairs	48 mA	1 nsec	50	5 pF
PCI-X microprocessor, 28 drivers	Memory I/O 3.3V	46[1] power/ground pairs	4 mA	1 nsec	50	8 pF
Five PCI-X microprocessors, 996 drivers	Core 1.8V	13 power/ground pairs	64 mA	1 nsec	50	8 pF
29LV040B, EEPROM			12 mA	5 nsec	100	8.5 pF
24C32, serial EEPROM			2 mA	1 µsec	100	8 pF
CY37064VP44-100ACCPLD, two power/ground pairs			12 mA	12 nsec	100	10 pF
Dual low-dropout regulators, TPS70351, 3.3V, 1.8V			1.5A (1.8V) 0.75A (3.3V)	1 µsec 1 µsec	77 79	47 µF 47 µF
Palce16C8Z			6 mA	5 nsec	100	8 pF

Notes:
Refer to tables 3, 4, and 5 for decoupling capacitance per power/ground pair.
[1]All sharing the same A7-chip power ring.

Using **Equation 1** and a 74-VHC1G04 chip, for example, with a gate capacitance of 3 pF, a dt of 1 nsec for t_R or t_P, and a maximum noise voltage of 50 mV:

$$\Delta I_{PER\ GATE} = 3\ pF\frac{50\ mV}{1\ nSEC} = 0.00375A. \quad (2)$$

The per-gate information is often unavailable, so a per-pin calculation works just as well. Each pin generally has a drive-cell macro behind it that you can treat as a pseudocell. Using a 74LVC04 as a step up in complexity, the results would be:

$$\Delta I_{PER\ PIN} = 5\ pF\frac{2.7V}{1\ nSEC} = 0.0135A,$$
$$\text{or } \Delta I_{PER\ PIN} = 5\ pF\frac{0.135V}{1\ nSEC} = 0.00068A. \quad (3)$$

The first number, 13.5 mA, is for current drawn for each full voltage switch per pin; the second number, 0.68 mA, indicates the voltage droop, 5%, that causes noise-current draw from across the power planes per pin, gate, or power bus. Therefore, ΔI for the whole chip equals ΔI times the six drive pins, or 81-mA, and the switching-noise (5% voltage droop) current is 4.1 mA for a 74LVC04.

Next, you need to determine the maximum power-bus impedance, because a digital system sees noise as voltage, or $\Delta I \cdot Z = \Delta V$. Therefore, you now have

$$\Delta Z = \frac{\Delta V_{NOISE\ MAX}}{\Delta I}, \quad (4)$$

which gives maximum impedance. From this **equation**, you can look for f_{PB}, the point at which $1/\omega C_D$ and ωL_B cross (**Figure 1**). At f_{PB}, the decoupling capacitors must begin working as high-frequency shorts and current supplies. The f_{PB} point indicates when impedance starts switching to an inductive impedance, which limits the responsiveness of the power bus to high-frequency power needs. The last parameter, ωL_D, is the shifted inductance line that the decoupling creates. Point f_{PD} is the place at which the inductance moves the system impedance back above the point at which current draw creates more voltage noise than is acceptable in the system. Z_{BUS} is the impedance of the power bus, which includes the power planes in a printed-wiring board.

Now that you know the origin of the remaining parameters, work toward C_D, which is the capacitance value that you need for the power/ground pairs on the chip that you are working to decouple. Using **equations 3** and **4**, you can calculate C_D from the following:

$$C_D = \frac{1}{2f_{PB}Z_{MAX}\pi}. \quad (5)$$

The last step is to make sure that C_D will work from f_{PB} to f_{PD} and is achievable for the needed high-frequency decoupling range.

Now, go back to the 74LVC04-chip example. The chip is a CMOS hex inverter. The di for a 74LVC04 at a V_{CC} of 2.7V has a 12-mA maximum output per driver from the data sheet. Assuming a 10 to 90% window, dv is 2.16V, and the assumed switching time is 1 nsec. Therefore, the minimum decoupling capacitance for the 74LVC04 is:

$$C_{MIN} \approx \Delta I \times \Delta T/\Delta V \approx \frac{72\ mA \times 1\ nSEC}{2.16V} \approx 33\ pF. \quad (6)$$

However, you need to take care of the voltage droop or noise that the driver current surge causes. So, the ΔV should be 50

TABLE 2 CHIP-DECOUPLING PARAMETERS

Chip	ΔI total	Δt	ΔV_{NOISE}
40-MHz oscillator, 3.3V	2 mA	1 nsec	50 msec
PCI-X microprocessor	3.3V, 0.2 mA 1.8V	0.8 nsec 1 nsec	50 mV 50 mV
29LV040B, EEPROM	12 mA	5 nsec	100 mV
24C32, serial EEPROM	2 mA	1 µsec	100 mV
CY37064VP44-100AC CPLD	12 mA	12 nsec	100 mV
Dual low-dropout regulators, TPS70351, 3.3V, 1.8V	1.5A, 1.8V 0.75A, 3.3V	1 µsec 1 µsec	77 mV 79 mV
Palce16C8Z	6 mA	5 nsec	100 mV

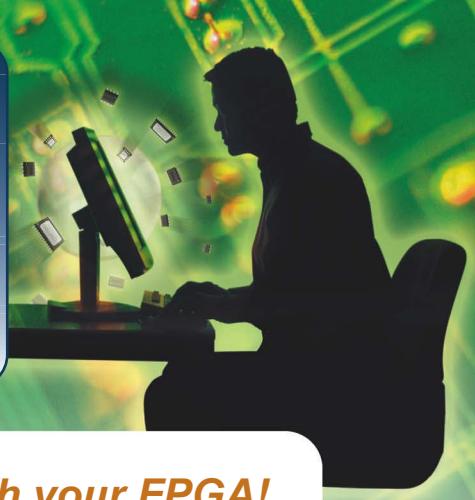
Note: Refer to tables 3, 4, and 5 for decoupling capacitance per chip.

TABLE 3 HIGH-SPEED-BYPASS-CAPACITANCE NEEDS FOR PCI SCSI BOARD

Component	ΔI per power-ring section	ΔI per pin	ΔT rise/fall fastest edge (sec)	ΔV_{MAX} (V)	Minimum capacitance per chip section	No. of active driver pins	No. of power/ground pairs	No. of 0.01-µF capacitors needed	Exact value in 0.01-µF capacitors
PCI-X microprocessor	0.6	0.016	2.5×10^{-9}	0.05	3×10^{-8}	96	46[1]	Three	3
PCI-X microprocessor	0.6	0.008	1×10^{-9}	0.05	1.2×10^{-8}	NA	13	Two	1.2
PCI-X microprocessor	0.2	0.048	1×10^{-9}	0.05	4×10^{-9}	Eight	Four	One	0.4
PCI-X microprocessor	0.6	0.004	4.8×10^{-9}	0.05	4.8×10^{-8}	29	46[1]	Five	4.8
CY37064VP44-100	0.171	0.0045	6×10^{-9}	0.05	2.05×10^{-8}	38	Eight	Three	2.052
Palce16C8Z	0.027	0.0045	6×10^{-9}	0.05	3.24×10^{-9}	Six	One	One	0.324
24C32	0.0045	0.0045	3×10^{-7}	0.05	2.7×10^{-8}	One	One	Three	2.7
29LV040B	0.036	0.0045	2.5×10^{-9}	0.05	1.8×10^{-9}	Eight	One	One	0.18
40-MHz oscillator	0.002	0.002	1×10^{-9}	0.05	4×10^{-11}	One	One	One	0.004

Notes: Total capacitance needed: 1.47×10^{-7}.
[1]All sharing the same chip power ring and power/ground pairs.

Design with Flexibility



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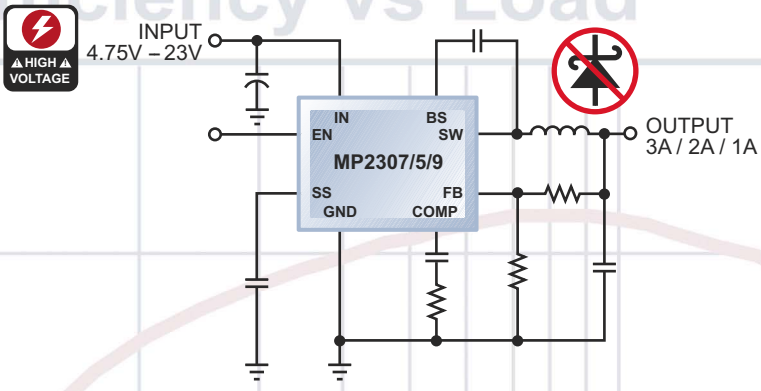

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mV for this example. This value gives you a minimum capacitance of:

$$C_{MIN} \approx 72\ mA \times 1\ nSEC / 50\ mV \approx 1.44\ nF. \quad (7)$$

This one sample chip could be on a board with 20 or 30 chips—from a simple 74LVC04 to Pentium-class chips with hundreds of pins or bond-out attachments. If more advanced software is not close at hand, a spreadsheet is the best way to obtain the total board capacitance and number of needed capacitors.

As a final example, work through the calculations for a generic PCI-X board with chips having well-defined parameters and a number of different main and support chips. The main processor chip is a 133-MHz PCI-X chip with a 3.3V I/O ring and 1.8V core, using a 40-MHz oscillator. Support chips are a 29LV040B EEPROM, dual low-dropout voltage regulator to supply 3.3 and 1.8V; a Palce16C8; one two-wire serial 24C32 EEPROM; and a CY37064VP44 CPLD. For each of these chips, you need to locate the current drive for each driver pin; determine the signal rise time, or Δt; and decide on the maximum noise voltage. Once you have chosen the decoupling capacitance, you can use the following equations to ensure that the impedance is not excessive and that the system does not have a resonance point:

$$Z_C = \sqrt{L/C}, \text{ and } f_O = \frac{1}{2\pi\sqrt{LC}}. \quad (8)$$

Table 1 covers the processor-chip board-decoupling parameters and per-chip board-decoupling capacitance needs.

So far, this article has focused on the lowest level (closest to the driver) or highest frequency of decoupling on a printed-wire assembly or circuit module—namely, the immediate quick-response current drawn for the chip at 1 MHz and greater frequencies, where t_R or t_F is 1 msec or less. However, bypass and decoupling need to occur at three levels of current-frequency draw for planned decoupling, with each of the levels requiring that the impedance be less than 1Ω for the best current-surge response and lowest noise or jitter characteristics at the chip and system levels. At the first level, the high-frequency quick-current surge associated with the digital-state and signal-I/O driver changes either on or off chip. The two other levels are the middle- and low-frequency ranges. Both ranges are resupply points to the next lower level of current-frequency bypass or decoupling.

MIDFREQUENCY COMPONENT LEVEL

Designers generally view the midfrequency range of tens to hundreds of kilohertz as a board-level issue or intermediate current- and voltage-supply depot. The intermediate bypass capacitors supply the chip-level decoupling capacitors with their immediate-need surge-current resupply through relatively low-inductance paths. The midrange bypass capacitors tend to have an inductance path at least an order of magnitude larger than the inductance path between the chip-level decoupling capacitors and the chips they supply. This tendency results in a response time for the midrange bypass capacitance that is close to an order of magnitude higher than the response time of the chip-level decoupling capacitors, with capacitor values in the single- to low-double-digit microfarad range of values.

The midrange is at a chip level. So what is Δt? The PCI-X microprocessor chip has core, memory, and PCI-X operating blocks, each of which has a different Δt or operating frequency.

READ MORE ABOUT IT

This article makes many assumptions and simplifications for developing a workable approach to finding the value of decoupling capacitance at the levels that most often exist on a pc-board assembly. For more precise details and information, please see the following sources:

Hall, Stephen H, Garrett W

1 Hall, James A McCall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*, ISBN 0-471-36090-2, John Wiley & Sons, 2002.

2 Van Doren, Thomas P, "Circuit Board Layout to Reduce Electromagnetic Emission and Susceptibility" seminar, IEEE EMC Fest, 2004.

3 Roy, Tanmoy, Larry Smith, and John Prymak, "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications," *Proceedings of the Seventh Topical Meeting on Electrical Performance of Electronic Packaging*, 1998, www.qsl.net/wbbtpu/si-list6/att-1775/01-ESR_ESL.pdf.

4 Brooks, Douglas, "ESR and Bypass Capacitor Self Resonant Behavior, How to Select Bypass Caps," Ultra CAD Design Inc, 2000, www.ultracad.com.

5 O'Hara, Martin, *EMC at Component and PCB Level*, ISBN 0-7506-3355-7, 1998.

6 Chen, Juan, Minjia Xu, Todd Hubing, James Drewniak, Thomas P Van Doren, Richard E DuBroff, "Experimental Evaluation of Power Bus Decoupling on a 4-Layer Printed Circuit Board," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility 2000, Volume 1*, pg 335.

7 Hubing, T, Thomas P Van Doren, F Sha, J Drewniak, and M Wihelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility 1995*, pg 308.

8 Fan, Jun, James L Knighten, Antonio Orlandi, Norman W Smith, James L Drewniak, "Quantifying Decoupling Capacitor Location," *Proceedings of IEEE International Symposium of Electromagnetic Compatibility 2000, Volume 2*, pg 761.

9 Radu, S, RE DuBroff, TH Hubing, Thomas P Van Doren, "Designing Power Bus Decoupling for CMOS Devices," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility 1998, Volume 1*, pg 375.

AT HIGH FREQUENCIES, THE PCI-X MICROPROCESSOR CHIP NEEDS 11 0.01-µF CAPACITORS; YOU COULD FURTHER DIVIDE THESE CAPACITORS INTO VALUES OF 0.01 µF, 1000 pF, AND 110 pF.

The correct Δt is the slowest one. It gives the minimum capacitance that is large enough to pass all frequencies of concern in the midrange (**Table 2**).

LOW FREQUENCY AND POWER RAILS

The low-frequency, or bulk-decoupling, range is associated with the power-supply bus, which connects the system/board power supply to the system and onto the board through either edge fingers or cable/wire connections. This bus usually has noise from a few hertz to 10 or 20 kHz, with a voltage and current ripple that you must consider when specifying parts. At this level, the value of capacitance is in either the hundreds or the thousands of microfarads.

Also at this level, you want to make sure that the power-bus impedance is low enough for the total board current draw (ΔI_{TB}) and the maximum voltage-noise budget. To determine this information, you need to know X_{MAX}, which is equal to $\Delta V_{NOISE\ MAX}/\Delta I_{TB}$. Once you know the maximum impedance, you need to estimate, calculate, or measure inductance for the power-supply rail leading up to the board. You can use this power-rail inductance, L_{PS}, to find the total capacitance the board needs to determine X_{MAX}. You can also use the L_{PS} to calculate the power-rail frequency needed to arrive at the total board capacitance.

RESULTS

Tables 3 through **5** show the results for high-, middle-, and low-frequency capacitance calculations on the PCI-X HAB (host-adapter-bus) board. At high frequencies, the PCI-X microprocessor chip needs 11 0.01-µF capacitors. In practice, you could further divide these capacitors into values of 0.01 µF, 1000 pF, and 110 pF, to give a number sufficient for one decoupling capacitor per two power/ground-pin pairs. This step minimizes the via and plane inductance in an attempt to keep the impedance from the capacitors to the power pin as far below 1Ω as possible. However, you must also stay within the necessary amount of capacitance and use a minimal number of capacitors. Three values help hold the response curve as flat as possible across the high-frequency spectrum. You should not place the capacitors next to each other in a parallel arrangement, because doing so dampens the effectiveness of the very-low-value capacitor. One practical side

TABLE 4 MIDSPEED-BYPASS-CAPACITANCE NEEDS FOR PCI SCSI BOARD

Component	ΔI per chip	ΔT rise/fall slowest edge for chip (sec)	ΔV_{MAX} (V)	Minimum capacitance per chip (µF)	No. of active driver pins on chip	No. of power/ ground pairs	1-µF capacitors needed	Exact value in 1-µF capacitors
PCI-X microprocessor	1.4	2.5×10^{-9}	0.05	7×10^{-8}	133	59	One	0.07
CY37064VP44-100	0.171	6×10^{-9}	0.05	2.05×10^{-8}	38	Eight	One	0.02052
Palce16C8Z	0.027	6×10^{-9}	0.05	3.24×10^{-9}	Eight	One	One	0.00324
24C32	0.0045	3×10^{-7}	0.05	2.7×10^{-8}	Two	One	One	0.027
29LV040B	0.036	2.5×10^{-9}	0.05	1.8×10^{-9}	Eight	One	One	0.0018
40-MHz oscillator	0.002	1×10^{-9}	0.05	4×10^{-11}	One	One	One	0.00004

Notes: Total capacitance needed: 1.23×10^{-7}.
Chip level requires no per-pin current drive.

TABLE 5 LOW-SPEED-BYPASS-CAPACITANCE NEEDS FOR PCI SCSI BOARD

Component	ΔI per chip	ΔT rise/fall slowest edge on board (sec)	ΔV_{MAX} (V)	Minimum capacitance per chip	No. of active driver gates/ pins in chip	No. of power/ ground pins on chip	10-µF capacitors needed
PCI-X microprocessor	1.4	2.5×10^{-9}	0.05	7×10^{-8}	133	59	None
CY37064VP44-100	0.171	6×10^{-9}	0.05	2.05×10^{-8}	38	Eight	None
Palce16C8Z	0.027	6×10^{-9}	0.05	3.24×10^{-9}	Eight	One	None
24C32	0.0045	3×10^{-7}	0.05	2.7×10^{-8}	Two	One	None
29LV040B	0.036	2.5×10^{-9}	0.05	1.8×10^{-9}	Eight	One	None
40-MHz oscillator	0.002	1×10^{-9}	0.05	4×10^{-11}	One	One	None
Total board parameters	1.6405	1×10^{-9}	0.05				None

Notes: The board power/ground capacitance is 7.5 nF for one power/ground pair, assuming a 3.5×6.6-in. board with a relative dielectric of 4.3 and 3 mils of space between the power planes. In this case, the power/ground pair would have an inductance of either 178 or 51 pH, depending on the width and length orientation, where the length is 6.6 in., and the width is 3.5 in. for the smaller inductance. These two bits of information give an impedance for the board power/ground-plane pair of approximately 0.083, or 0.154Ω.
Total capacitance needed: 3.28×10^{-8}.
Board level requires no per-pin current drive.

benefit of knowing the correct amount of capacitance is that you can avoid overusing capacitors, which can open board-routing channels around large chips and reduce via count through power and ground planes.

You then need to calculate the total board bulk capacitance. Make sure that high, middle, and low ranges add up to a total that will give the capacitance value that will deliver the needed impedance for X_{MAX} for the power-supply rail: $X_{MAX}=\Delta V_{NOISEMAX}/\Delta I_{TB}$: From **Table 5**, $\Delta V_{NOISEMAX}=50$ mV, and $\Delta I_{TB}=1.64$A. $X_{MAX}=0.030\Omega$, and L_{PS} is 200 nH. So, $f_{PS}=X_{MAX}/2\pi L_{PS}=0.030/2\pi 200$ nH$=24$ kHz. Therefore, $C_{TB}=1/2\pi f_{PS}X_{MAX}=220$ µF.

The total capacitance from **tables 3**, **4**, and **5** is 1.62 µF. So, the board needs 220 µF for bulk capacitance to pull the power-supply-rail impedance up to 0.030Ω. This value is large for a board that is the size of a normal PCI plug-in card. You should therefore review issues that can affect the value for the bulk capacitance if this amount of bulk decoupling will be a problem.

A ΔV, voltage droop, or jitter factor of 50 mV might indicate that the analysis is too stringent, so you should look at other ways to lower the power-supply-rail inductance to reduce the bulk decoupling to a smaller value. Changing ΔV to 100 mV moves C_{TB} to 54 µF. This change, however, makes the invalid assumption that only this card is on the PCI power rail. You can achieve the same effect by reducing the power-supply-rail inductance to 100 nH.

The key parameter for specifying a more appropriate amount of decoupling capacitance is keeping the current-supply bus impedance between the bulk capacitors and the power supplies below 1Ω. The lower the impedance, the better your chance of minimizing the voltage noise or jitter that the 0Ω, nonideal power-bus impedance generates.

A critical topic that this article does not cover is the impedance between the decoupling/bypass-capacitor placement and the attachment methodologies. The best capacitor-attachment approach is to use surface-mount components with vias in pads to create small inductance-loop areas and, thus, small inductance values to minimize the impact on path impedance. EDN

AUTHOR'S BIOGRAPHY

Barry Caldwell is a senior member of the IEEE EMC Society with Narte Certifications in EMC and ESD. He holds more than 20 patents, including those for EMC and high-speed-compensation technologies. He currently spends his working hours on joint Adaptec and Vitesse projects but plays par-three golf, given the chance. You can reach him at barryc@vitesse.com.

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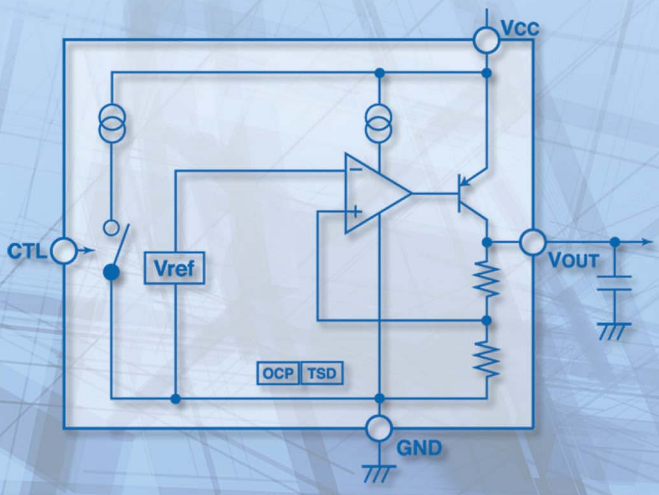

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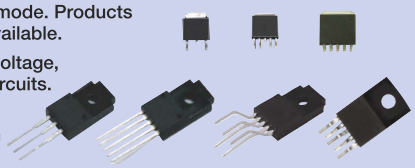

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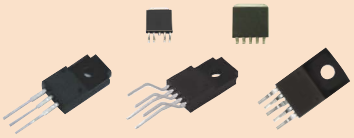

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BD00KA5W series

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Input voltage: up to 18V
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BA□□BC0 series in all 50 models

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BD00BC0W series

Output: 1.5A
Input voltage: up to 18V
Output: 1.5・1.8・2.5・3.0・3.3・5.0・6.0・6.3・8.0・9.0・10.0V
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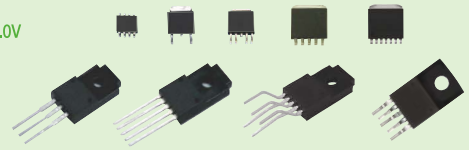

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Output: 150mA・Input voltage: up to 5.5V
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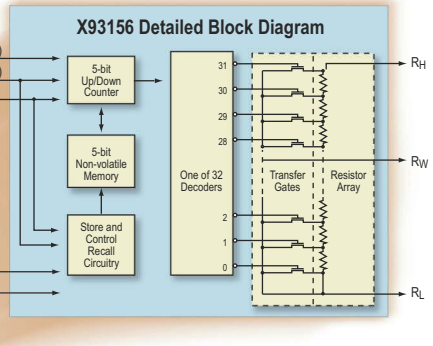

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R_H, R_L Terminal Voltages		0	-	V_{CC}	V
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Wiper Current		-	-	0.6	mA
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Move to 12V bus eliminates need for isolated dc/dc converters

THE PART AND COST REDUCTIONS OF THE LOWER VOLTAGE, 12V BUS OUTWEIGH THE BENEFITS OF THE HIGHER VOLTAGE, 48V BUS.

Powering the ICs scattered on and across the multiple pc boards in a system has always presented challenges to power-supply designers. As long as the required voltages were relatively high, it was possible to locate the power conversion in a remote area of the system, where thermal and noise management was easier. However, as the required voltages decreased, power-conversion devices moved closer and closer to the usage points of power.

This migration from multiple output-power supplies, driven by the lower voltage and higher current requirements of the latest microprocessors, has reached a point at which today's systems exclusively use a single 48V front-end power supply with final conversion to the lower voltages done on the pc board. The increasing converter-power densities and the resulting converter-size reductions are major reasons for the rapid adoption of a distributed-power architecture (**Table 1**).

The next emerging trend, driven by technology-conversion advances and cost considerations, is the shift from a 48V to a 12V distribution bus and the resulting elimination of the onboard isolated dc/dc converter.

Several parameters—including the need for battery backup, the overall system-power level, device efficiency, copper-trace losses, connector consideration, and overall system cost—will drive your decision to use either one of the distribution voltages, and you should examine each new system design for the optimal approach.

48V BUS AND IBA

In 48V systems, an ac/dc front end or, in the case of battery backup, an ac/dc rectifier to the 48V-distribution-bus voltage converts the input ac. An isolated dc/dc converter further converts the bus voltage on each pc board to an intermediate-bus voltage and distributes it on the board to individual nonisolated POL (point-of-load) converters powering the ICs. Such design is commonly called an IBA (intermediate-bus architecture, **Figure 1**).

The distribution of a higher 48V-bus voltage at lower currents allows for smaller traces and connectors. Because the output Schottky-rectifier-diode drops are small fractions of the output voltage, 48V front ends can be efficient and cost-effective. Distribution of the higher voltages reduces the need for heavy cop-

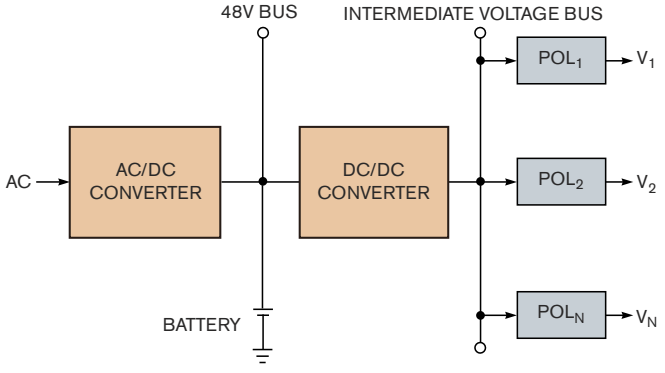

Figure 1 IBA relies on a 48V bus to distribute power to take advantage of the lower current and smaller circuit traces for power distribution, with separate point-of-load dc/dc converters to drop the voltage to 12V.

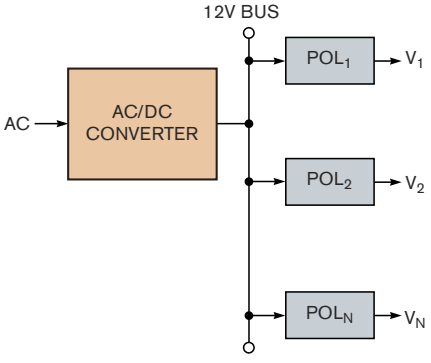

Figure 2 In a 12V-bus architecture, the single 12V bus eliminates the need for the intermediate 48V conversion, but the higher currents of the lower voltage 12V distribution systems result in heavier traces and bus bars.

TABLE 1 CONVERTER-POWER DENSITIES AND RESULTING CONVERTER-SIZE REDUCTIONS

Model	P_{OUT} (W)	V_{OUT} (V)	Size ($in.^3$)	Power density ($W/in.^3$)	I_{OUT} (A)
SPM5	1500	48	440	3	31
FNP1500	1500	48	99	15	31
FNP850	850	12	62	14	71

TABLE 2 CONSIDERATIONS FOR CHOOSING A 48 OR A 12V BUS

	12V bus		48V bus	
Consideration	Advanced	Distributed	Advanced	Distributed
Cost	X			X
Area	X			X
Efficiency	X			X
Connector		X	X	
Current		X	X	

TABLE 3 CURRENT VERSUS TRACE WIDTH (IN.)

Current (A)	20°C		30°C		50°C	
	1 oz	3 oz	1 oz	3 oz	1 oz	3 oz
1	0.007	0.003	0.005	0.002	0.004	0.001
10	0.2	0.065	0.15	0.05	0.1	0.035
20	0.5	0.18	0.38	0.13	0.27	0.09
30					0.55	0.18

per traces, or bus bars, and special high-current connectors, thus saving both system cost and space. However, the pc board still needs a secondary conversion by a dc/dc converter to the lower voltages that the POLs require.

You must compare the penalties of lower overall efficiency—due to the three conversion stages and the cost and pc-board space resulting from the additional 48 to 12V dc/dc converters—with the benefits of power transmission at the higher voltages.

WHEN A SYSTEM REQUIRES BATTERY BACKUP, THE 48V BUS IS THE OBVIOUS CHOICE. HOWEVER, FOR SYSTEMS USING LESS THAN 3000W, THE 12V BUS IS GAINING GROUND.

12V BUS BENEFITS FROM AC/DC EFFICIENCY

With the widespread adoption of synchronous rectification, the increased efficiency of ac/dc conversion has enabled 12V-output front-end power supplies to be as efficient as higher voltage output converters.

Designs that require no battery backup can effectively use the 12V bus to directly supply 12V to each pc board. Because the ac/dc front ends provide basic system isolation, you can eliminate additional isolation on the board and channel the 12V bus directly to the individual POLs (**Figure 2**).

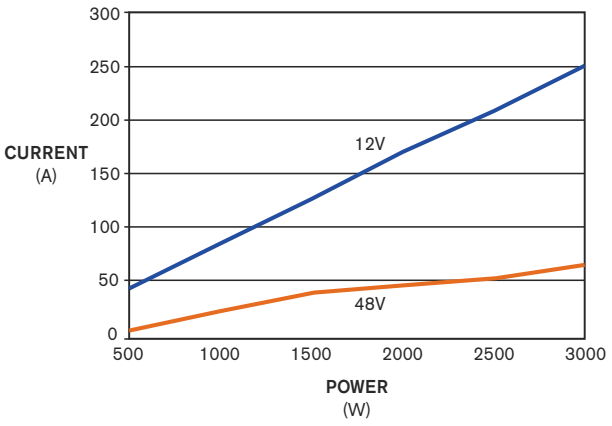

Figure 3 Although at power levels higher than 3000W, a 48V bus usually is a better choice, the 12V bus is gaining ground for systems using less than 3000W, requiring heavier pc-board traces to carry the higher currents. For example, a 3000W system at 12V has 250A distributed across the system.

The trade-offs of the lower voltage distribution are the requirements for higher distribution currents and the resulting need to use heavier pc-board traces and bus bars.

48V VERSUS 12V BUS

So, how do you decide which bus level to use? Although there are many factors to consider, system-power level can be a quick starting point in the selection process (**Table 2**).

When a system requires battery backup, the 48V bus is the obvious choice. At the power levels higher than 3000W, the 48V bus is usually a better choice. However, for systems using less than 3000W, the 12V bus is gaining ground.

As **Figure 3** shows, 3000W at 12V would require that 250A be distributed across the system. Distributing such high currents requires serious consideration for proper power-distribution methods. Factors include the number of pc boards in a system, the overall system-bus-distribution schemes, the required pc-board-trace widths, and the need for heavier pc-board bus-bar arrangements.

Mainframe computers have for many years used such power-distribution methods. Distribution of high currents on the pc board itself is a fairly recent development. Higher current distribution on the pc board requires wider traces, thicker copper, and consideration for extra layers (**Table 3**). Proper airflow on the pc board is also a big factor in reducing the trace widths.

Connections to the pc board are other important considerations with higher currents. New connector designs that can accommodate such high currents are currently available. EDN

AUTHOR'S BIOGRAPHY

HR Modi is director of strategic marketing, ac/dc, at Power-One, where his responsibilities include developing new business, the company-product road map, and customer interface. His interests cover reading, community work, playing the electronic keyboard, and teaching math.

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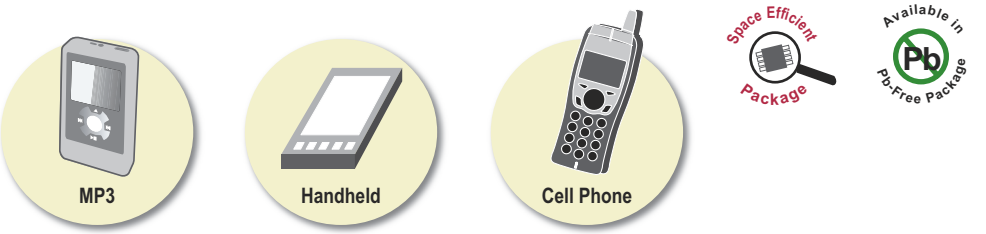
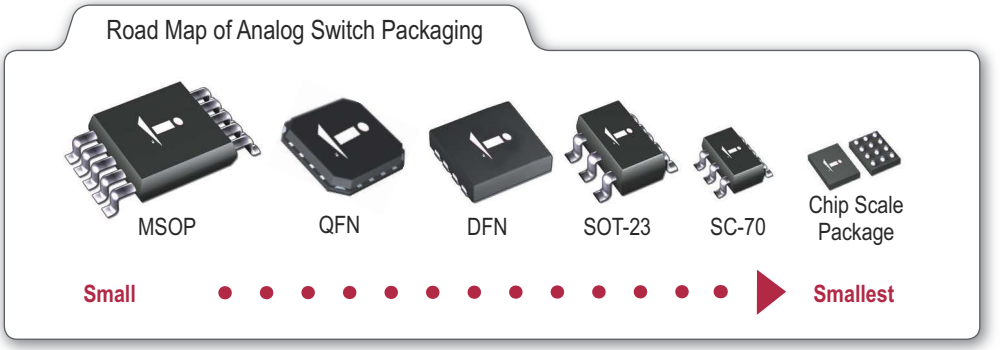
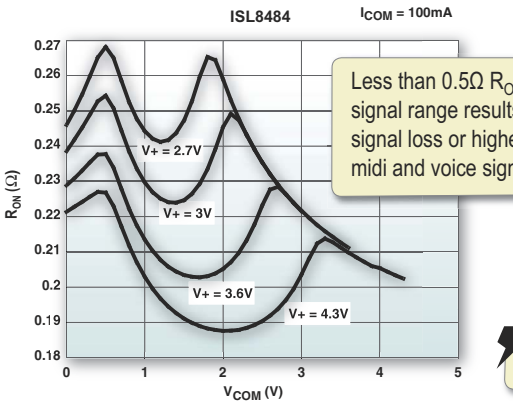
9kV ESD-protected, +1.1V to +4.5V, single supply, dual SPDT switches ensure reliability in handheld applications.

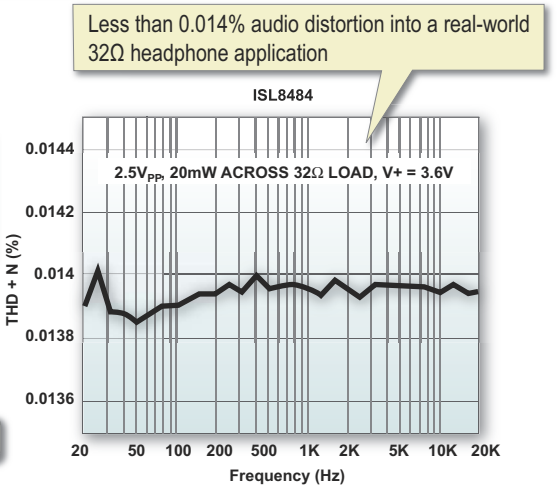






ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

9kV ESD HBM

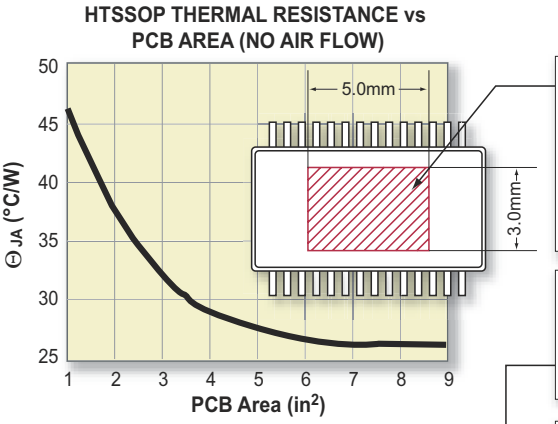


DISTORTION vs FREQUENCY

Device	Switch or MUX	Configuration	Type of Switch	$r_{DS(ON)}$ (Ω)	$T_{(ON)}$ (ns)	$T_{(OFF)}$ (ns)	CHG INJ (pC)	Leakage (nA)	SRC Cap (pF)	DRN Cap (ON) (pF)	I_{CC} (nA)	V_{CC} Range (±V)	Package
ISL8484	Switch/MUX	Dual 2x1	SPDT	0.27	20	15	128	0.01	115	224	80	+1.65 to +4.5	10 Ld DFN, 10 Ld MSOP
ISL8499	Switch/MUX	Quad 2x1	SPDT (Dual DPDT)	0.26	15	13	120	0.01	106	212	80	+1.65 to +4.5	16 Ld QFN, 16 Ld TSSOP

DC/DC Buck Regulators with Integrated FETs Resist Heat

Available in Pb-Free Package

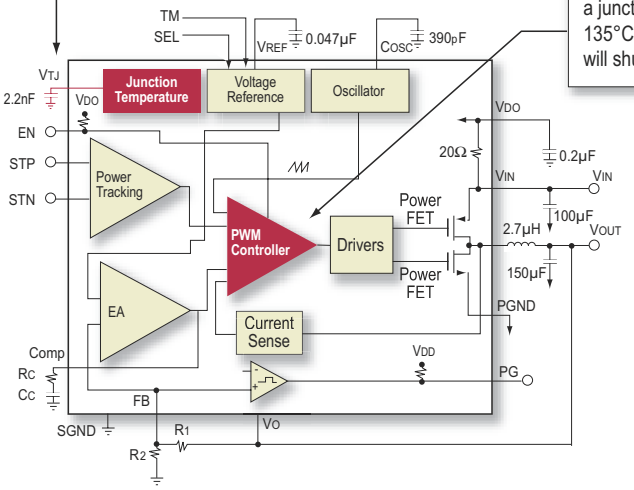


The first line of defense against heat is a thermally-efficient HTSOP-28 package, which utilizes an exposed thermal pad underneath the IC to spread heat through the PCB.

The V_{TJ} pin is a formula-based, accurate indicator of the internal silicon junction temperature.

If all else fails and the temperature sensor indicates a junction temperature above 135°C, the PWM Regulator will shut down.

Built-in thermal protection and voltage margining for actual in-circuit performance validation.



Key Features:

- 4A (EL7554) and 6A (EL7566) continuous output current
- Up to 96% efficiency
- Built-in 5% voltage margining
- 3V-to-6V input voltage
- 0.58 in² (EL7554) and 0.72 in² (EL7566) footprint with components on one side of PCB
- Adjustable switching frequency to 1MHz

Key Specifications

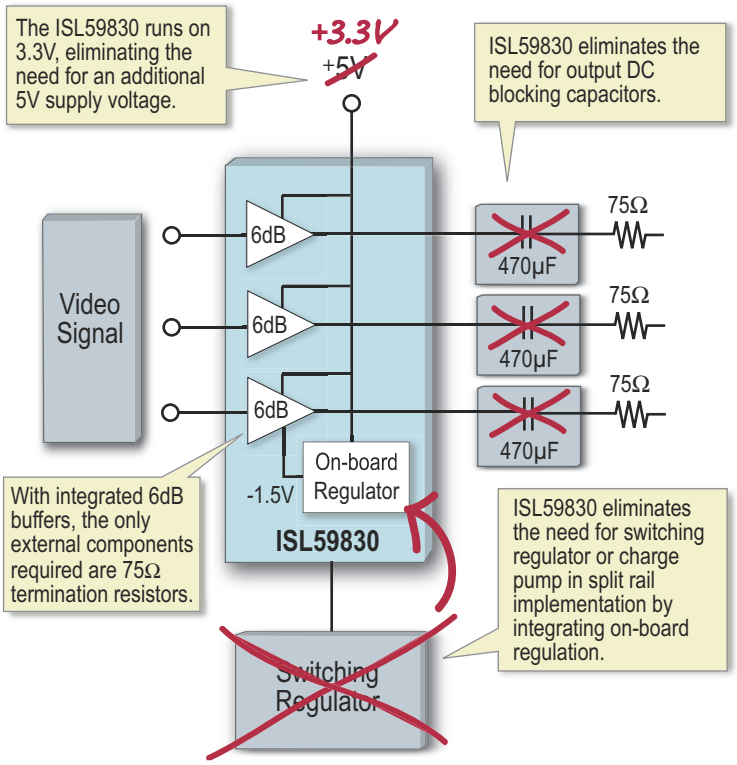
Device	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	Freq.	Efficiency	BOM Total Footprint	Package
EL7554	3	6	0.8	V_{IN}	4	200kHz to 1MHz	95%	0.8 x 0.72	28 Ld HTSSOP
EL7566	3	6	0.8	V_{IN}	6	200kHz to 1MHz	95%	1 x 0.72	28 Ld HTSSOP

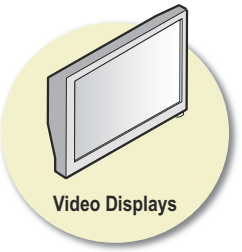
Eliminate Extra Voltage Supply with Integrated Triple +3.3V Video Buffer

The ISL59830 triple video buffer delivers DC-accurate coupling of video onto a 75Ω double-terminated line, and 300MHz of -3dB bandwidth performance.

Available in Pb-Free Package

ISL59830 Functional Block Diagram





Key Features:

- Triple single-supply buffer
- Operates from single +3.3V supply
- Eliminates need for DC blocking capacitors
- Fixed gain of 2 output buffer
- Output 3-statable
- Enable/disable functions
- 50MHz 0.1dB bandwidth
- 300MHz -3dB bandwidth

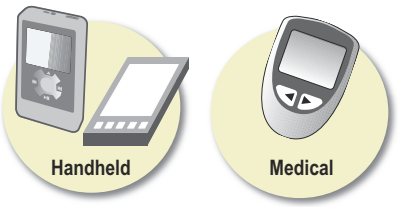
Key Specifications

Device	# of Amps	BW @ -3dB (MHz)	Slew Rate (V/µs)	V_S (min) (V)	V_S (max) (V)	V_N (nV/√Hz)	Rail-to-Rail	Gain A_V (min) (V)	I_S (per amp) (mA)	I_{BIAS} (µA)	I_{OUT} (mA)	V_{OUT} (V)	Diff Gain (%)	Diff Phase (°)	V_{OS} (max) (mV)	CMRR (dB)	PSRR (dB)	Package
ISL59830	3	200	500	3.0	3.6	20	Y	2	50	N/A	50/ -18	-1.8 to 3.3	0.06	0.1	25	90	90	16 Ld QSOP

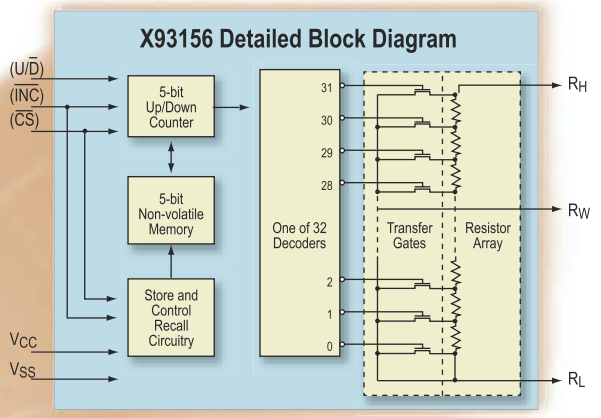
World's Smallest and Lowest Cost Non-Volatile Digital Potentiometer

The X93154, X93155 and X93156 address new market needs for high-volume and space-constrained applications such as portable or personal communications devices.

Available in Pb-Free Package



All this functionality in tiny 2mm x 2.5mm TDFN package



Key Features:

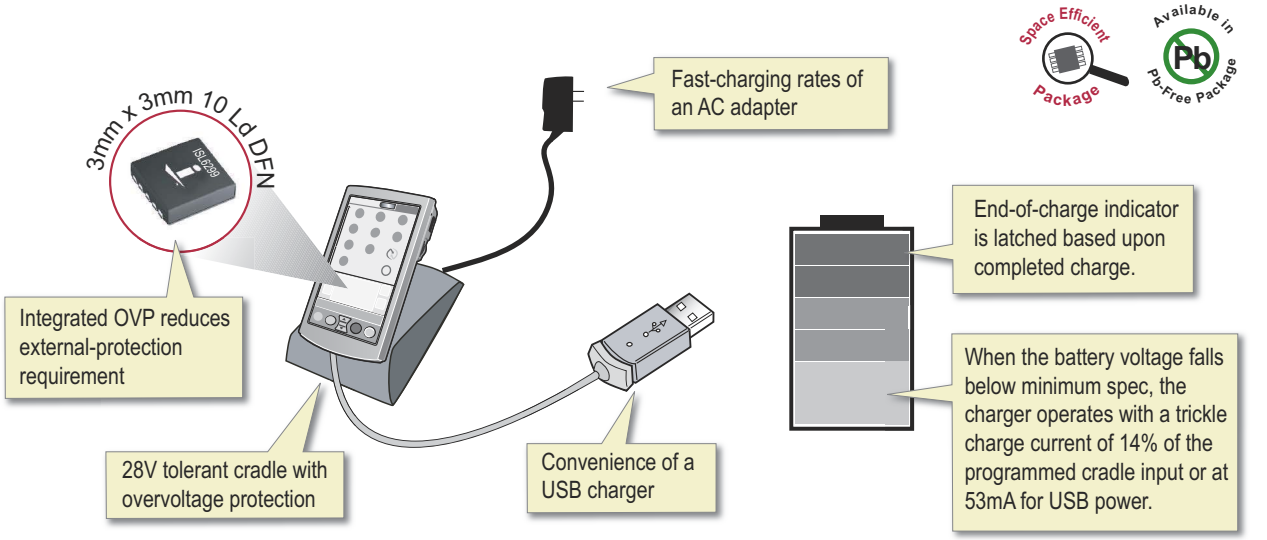
- 3-wire up/down interface
- 32 wiper tap points. Wiper position stored in non-volatile memory and recalled on power-up
- Low power CMOS, with V_{CC} of 2.7V to 5.5V, active current of 250µA max, and standby current of 1µA max
- High reliability with endurance 200,000 data changes per bit and register data retention of 100 years
- Available in 8 Ld MSOP and TDFN packages

Key Specifications

Device	Memory Type	Interface Type	Resistance Options (kΩ)	Single Supply (V_{CC}, GND)	V_S Range 2.7V - 5.5V	V_S Range 3.0V - 5.5V	V_S Range 4.5V - 5.5V	Resistance Taper	V_L - V_H (V)	Wiper Current (I_W) (mA)	Wiper Resistance (RW @ I_W)	Standby Current Isb (µA)	Package
X93154	Non-Volatile	3-Wire (Up/Down)	50	X		X		Linear	0 to +3.0	±0.6	1kΩ @ 0.6mA	1	8 Ld MSOP, 8 Ld DFN
X93155	Non-Volatile	3-Wire (Up/Down)	50	X			X	Linear	0 to V_{CC}	±0.6	1kΩ @ 0.6mA	2	8 Ld MSOP
X93156	Non-Volatile	3-Wire (Up/Down)	12.5, 50	X	X			Linear	0 to V_{CC}	±0.6	1kΩ @ 0.6mA	1	8 Ld MSOP

HV Dual Input Battery Charger Simplifies Design

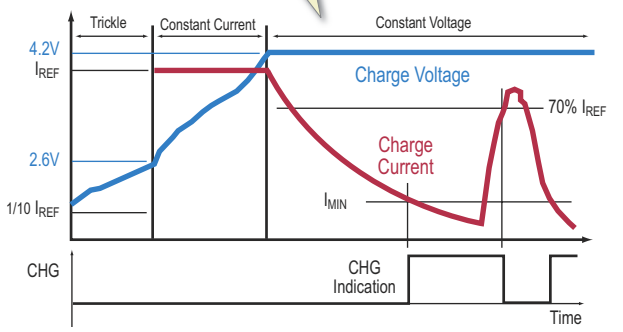
ISL6299 is a fully integrated, single-cell Li-ion / Li-Polymer battery charger with 28V tolerant input



Industry's Highest Input Voltage in the Most Compact Package

Intersil's ISL6294, single-cell Li-ion / Li-Polymer battery charger IC can handle input voltages up to 28V, eliminating the need for an overvoltage protection circuit

If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge the battery without the risk of overcharge.



TYPICAL CHARGE PROFILE

Available in Pb-Free Package

2mm x 2mm 8 Ld DFN Package

Key Features:

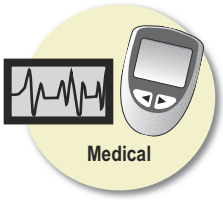
- 28V maximum input voltage
- Programmable end-of-charge current
- Thermaguard™ charge current thermal foldback for thermal protection
- No external blocking diode required
- Integrated pass element and current sensor
- 1% voltage accuracy

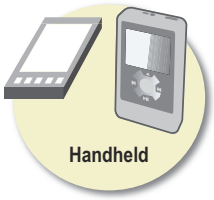
Real Time Clock with InterSeal™ Preserves Battery Life

The InterSeal™ battery saver seal prevents initial battery current drain prior to first use by switching to backup mode after first power up with less than 400nA typical power dissipation.

Space Efficient Package

Available in Pb-Free Package





11 Year Life Time

Intelligent Battery Backup Switchover
V_{DD} and backup source with intelligent switchover help to ensure continuous RTC operation and integrity of register and memory contents.

Key Features:

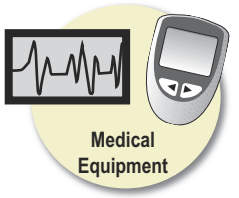
- The on-chip oscillator compensation allows on-the-fly frequency adjustment across temperature range.
- The flexible signal frequency output pin (IRQ output) functions both as an interrupt signal alarm for action or a user-selectable signal.
- ISL1209 event detection notifies and records “intrusion” time.

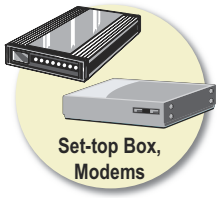
Key Specifications

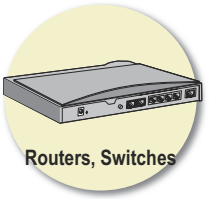
Device	V_{CC}	V_{BATT}	# of Alarms	Power-ON Reset	Watch-Dog Timer	Clock Freq Out	On-Chip OSC Temp Compensation	Batt Switch or Super Cap	IRQ Output	EEPROM Size (Bits) (K)	Package
ISL1208	2.7 to 5.5	1.8 to 5.5	1	N	N	Y	Y	Y	Y	16 Bits SRAM	8 Ld MSOP, 8 Ld SOIC
ISL1209	2.7 to 5.5	1.8 to 5.5	1	N	N	Y	Y	Y	Y	16 Bits SRAM	10 Ld MSOP, 18 Ld PDIP

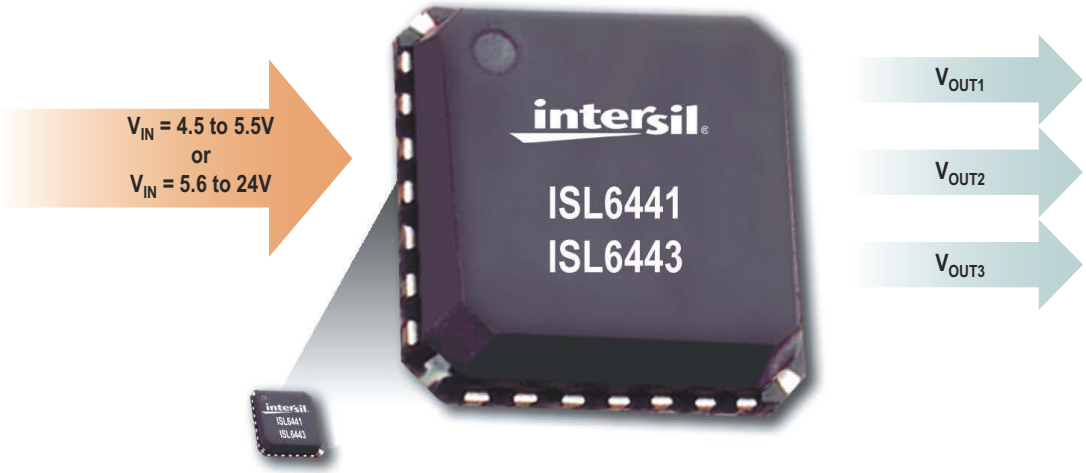
Triple Output Controllers Optimized for Multiple Rails

Available in Pb-Free Package









5mm x 5mm QFN

Key Features:

- Switching frequency of 1.4MHz (ISL6441) or 300kHz (ISL6443, ISL6440)
- Tiny footprint and excellent thermal resistance in QFN package
- Overcurrent and overvoltage protection
- Triple regulated output voltages for multiple rails

Key Specifications

Device	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT1} (min) (V)	V_{OUT1} (max) (V)	V_{OUT2} (V)	V_{OUT3} (V)	I_{OUT} (max) (A)	I_{OUT1} (A)	I_{OUT2} (A)	Switching Frequency	Package
ISL6440	4.5	24	0.8	24	N/A	N/A	10	N/A	N/A	300kHz	24 Ld QSOP
ISL6441	4.5	24	0.8	24	24	Adj.	N/A	20	20	1.4MHz	28 Ld QFN
ISL6443	4.5	24	0.8	24	24	Adj.	N/A	20	20	300kHz	28 Ld QFN

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The thermal conductivity of our eGraf® HS-400™ material, a proprietary composite of natural graphite, rivals copper by exceeding 370 W/m•K. Compare that to conductivities of the aluminum alloys commonly used in extruded heat sinks such as 6061 (166 W/m•K) and 6063 (201 W/m•K). This impressive thermal performance is made possible by the highly directional properties of eGraf® natural graphite.

To create a superior lightweight heat sink, eGraf® HS-400™ graphite fins are bonded to a metal base with a high thermal conductivity epoxy.

These bonding techniques, specially developed by GrafTech, insure excellent thermal performance, mechanical reliability and cost-effectiveness.

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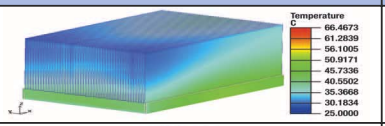
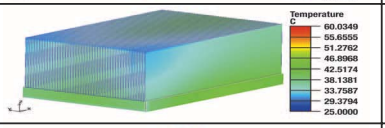
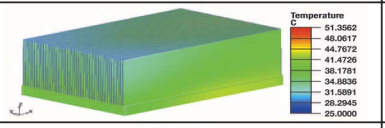
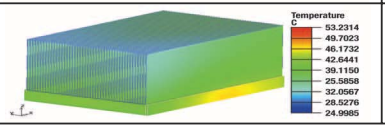
Graftech can custom design and thermally model heat sinks with any type of base design:

- Cu base/graphite fin
- Cu base w/ heat-pipes/graphite fin
- Al base/graphite fin
- Al base w/ heat-pipes/graphite fin

Heat Sink Comparison

Material Option	T_{max} (°C)	R_{sa} (°C/W)	Temperature Distribution	Weight (kg)
Base-Fin				
Al-Al	66.5	0.100		2.14
Al-HS-400™	60.0	0.084		1.79
Cu-Cu	51.4	0.063		6.47
Cu-HS-400™	53.2	0.068		3.62

Ambient Temperature: 25°C Chip Power: 416 W Airflow Rate: 100 m³/h Dimensions: 180x120x80 mm Base Thickness: 14 mm Fin Thickness: 0.75 mm Number of Fins: 46

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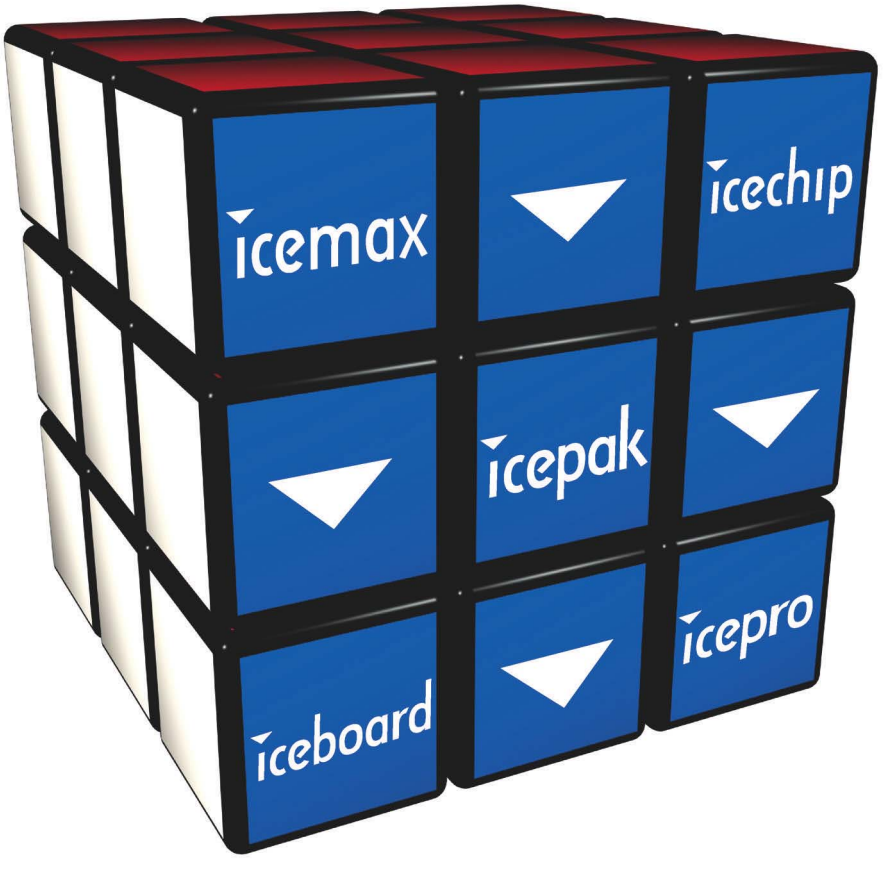

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BY SHAKER SARWARY, ATRENTA, AND MICHAEL A BEAVER, INSILICA

A systematic approach to verifying FSMs

CAREFUL ATTENTION TO MANAGING THE DESIGN-STYLE CHOICES AND COMPLEXITY ATTRIBUTES FOR FINITE-STATE MACHINES CAN IMPACT THE QUALITY AND VERIFIABILITY OF THE FINAL IMPLEMENTATION.

Large SOCs (systems on chips) comprise many FSMs (finite-state machines), which combine with datapaths, memories, and other components. Although FSMs are among the most abundant components on chips, many designers lack an understanding of their role and their impact on the quality and validation of the final chip implementation. FSMs are sources of functional bugs in SOCs. Designers often attribute poor timing, power, and performance to poor FSM design; therefore, FSM verifiability and FSM-design-style considerations are important aspects of SOC design. Although verification tools can perform checks on FSMs, such as deadlock and unreachable states, these tools may not consider the aspects of FSM-design styles (**Figure 1**). This article takes a predictive look at FSMs and discusses functional and implementation issues resulting from various FSM-design styles. It also provides guidelines for designing and implementing FSMs to meet design goals (**references 1** and **2**).

The most common functional problems in FSMs include unreachable or deadlocked states, dead transitions, constant registers, and asynchronous inputs. An unreachable state is one that the FSM cannot reach from any initial state, and it can indicate a functional problem in the design or result from an unintentional dead transition in the FSM. In any case, an unreachable state indicates redundant logic in the design that the designer should clean up. A dead transition is a transition that the FSM can never exercise; it also indicates redundancy in a design.

A deadlock state is a state from which the FSM cannot move to another reachable state. Similarly, an n-deadlock state is a set of n states in which all transitions from any of these states reach states only within the set. It is also possible that a transition occurs out of a state only for a finite number of times. This situation means that the FSM will eventually lock to this state. This type of deadlock state—"eventually deadlock"—may remain unidentified during simple verification and simulation but can cause serious failures on-chip. **Figure 2** shows an example of an eventually deadlocked state.

Another common condition occurs when an FSM register becomes stuck at a constant value of zero or one that is caused by FSM encoding, and it may indicate a wrong or suboptimal encoding. An asynchronous input is an FSM input coming from a clock domain other than the one controlling the state registers. This condition may arise from properly built, functional handshaking circuitry. However, designers should review any asynchronous inputs to ensure that an unsynchronized input does not cause any clock-crossing issues.

FSM METRICS

In addition to these problems, the FSM-design style may impact the verifiability of an FSM. Designers should analyze

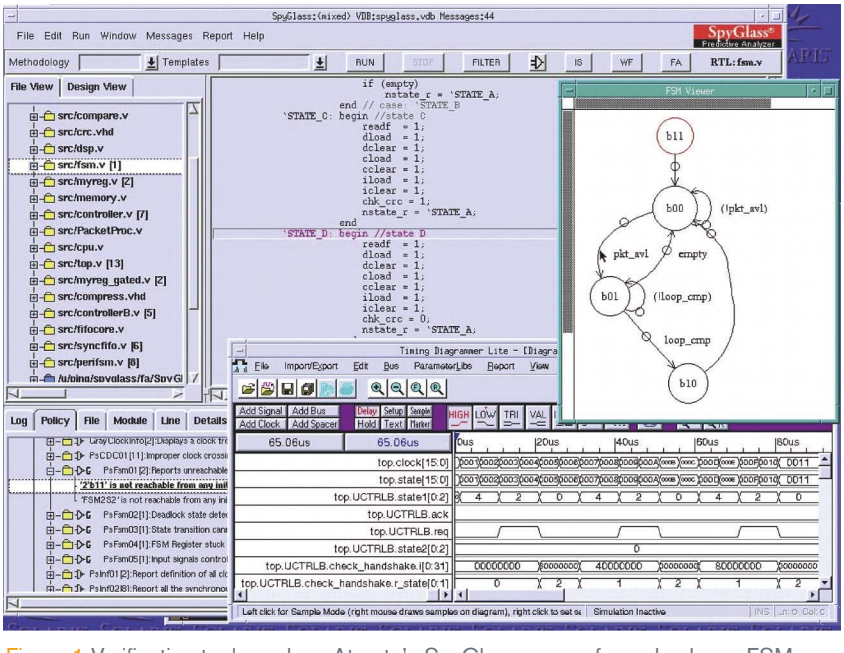
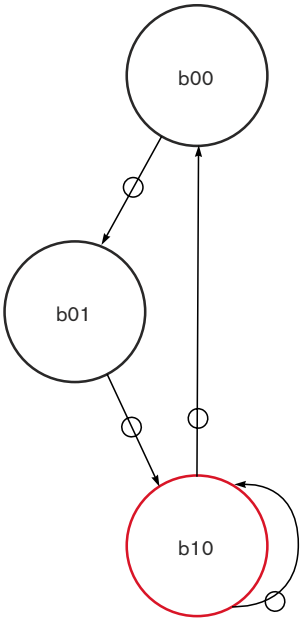


Figure 1 Verification tools such as Atrenta's SpyGlass can perform checks on FSMs, such as deadlock and unreachable states.

metrics to determine whether a given simulated or formal validation flow can verify the FSM. Designers can use FSM attributes, such as the number and depth of states, transitions, inputs, and outputs, to qualify an FSM from an implementation and verification point of view. These attributes can have a major impact on the quality of implementation of an FSM. Encoding styles, output, and next-state-logic descriptions, as well as the presence and description of the initial state, can affect the implementation and verification of an FSM.

The number of states is the first indicator of an FSM's complexity. A larger set of states can make the FSM code difficult to read, difficult to understand, and likely to contain functional bugs. A large number of states can complicate the FSM encoding, and it can contribute to extra combinational and sequential logic that incurs timing, area, and power penalties. Large FSMs make the validation effort more challenging and may lead to low verification coverage. Decomposing larger FSMs into smaller, communicating FSMs helps in all these areas. Keeping the number of states lower than 20 is a good FSM-coding practice.

The number of transitions in an FSM is another indicator of the FSM's complexity. Complex transitions can lead to complex next-state combinational logic, which can directly impact the timing. Similar to FSMs with a large number of states, an FSM with a large number of transitions increases the designer's effort to maintain, enhance, and verify that FSM. Reducing the number of transitions may require rebuilding a module with new




```
`define S0 2'b00
`define S1 2'b01
`define S2 2'b10
`define S3 2'b11


module fsm(clk, rst_n, out);

 input  clk;
 input  rst_n;

 output out;

 reg out;
 reg[1:0] cstate;
 //reg[1:0] nstate;
 reg [3:0] cnt;

 always @(posedge clk or negedge rst_n) begin
 if (~rst_n) begin
   cnt <= 0;
   cstate <= `S0;
   out <= 0;
   end
 else
   case (cstate)
     `S0: begin
       out <= 1'b0;
       cstate <= `S1;
       end
     `S1: begin
       out <= 1'b1;
       cnt <= cnt + 1;
       cstate <= `S2;
       end
     `S2: begin
       out <= 1'b0;
       if (cnt == 4'b0100)
         cstate <= `S2;
       else
         cstate <= `S0;
       end
   endcase
 end

endmodule
```

Figure 2 In an eventually deadlocked state, the FSM moves from State 2 to State 0 until the count reaches a value of 4. The FSM then locks in State 2.

MINIMUM ENCODING RESULTS IN THE MINIMUM NUMBER OF STATE REGISTERS, BUT THE CONTROL LOGIC MAY BE MORE COMPLEX.

control circuitry, but this technique results in more modular code that is easier to maintain and enhance. Typically, two transitions per state should be sufficient to express common functions in terms of an FSM. For a 20-state FSM, 40 transitions would occur.

The number of inputs to or outputs from an FSM impacts the complexity of the output and the next-state logic. As a rule of thumb, the number of inputs to an FSM should not exceed the number of states in an FSM. Typically, the number of outputs from an FSM should be small. For example, 25 outputs would help control complexity.

The depth of the FSM refers to the number of states on the longest path from an initial state without visiting the same state twice. Deep FSMs may be harder to verify, especially when they have a high number of states and transitions, which makes the FSM wide and deep. The FSM depth should be kept at less than 15 to enable a simpler verification and debugging process.

STYLES

The encoding style for an FSM has a high impact on the quality of the FSM implementation in timing, area, power, and other attributes. Some of the most common encoding styles include one-hot encoding, Gray encoding, and minimum encoding. The one-hot-encoding style means that only one bit of the state registers can be at one for any given state of the FSM. This encoding may result in a higher number of registers in the final implementation. The combinational-logic complexity resulting from one-hot encoding may be comparable or slightly more than other encoding styles, but the combinational logic controlling the data input of each state register may be smaller, which may contribute to better timing performance. A designer may choose this encoding style for its simplicity and its timing performance.

Gray encoding is a special state-encoding style in which source and destination states for any transition in an FSM have only one different bit in their encodings. Because a single register can change value during any transition, Gray encoding is the best choice for lower power consumption. The number of registers for encoding the states may be small, but the combinational-logic complexity for next-state and output generation is unpredictable. It may be difficult to find an optimal Gray-encoding scheme for large FSMs with many transitions.

Minimum encoding results in the minimum number of state registers, but the control logic may be more complex. A designer can minimize the combinational logic with carefully assigned encoding. Depending on the level of optimization in the encoding, this encoding style may result in good or poor timing and area performance. Unless a designer deploys an optimized encoding scheme, this encoding style may be a poor choice. Use it if the total number of registers in a design is a concern, but don't use it if power is the main concern.

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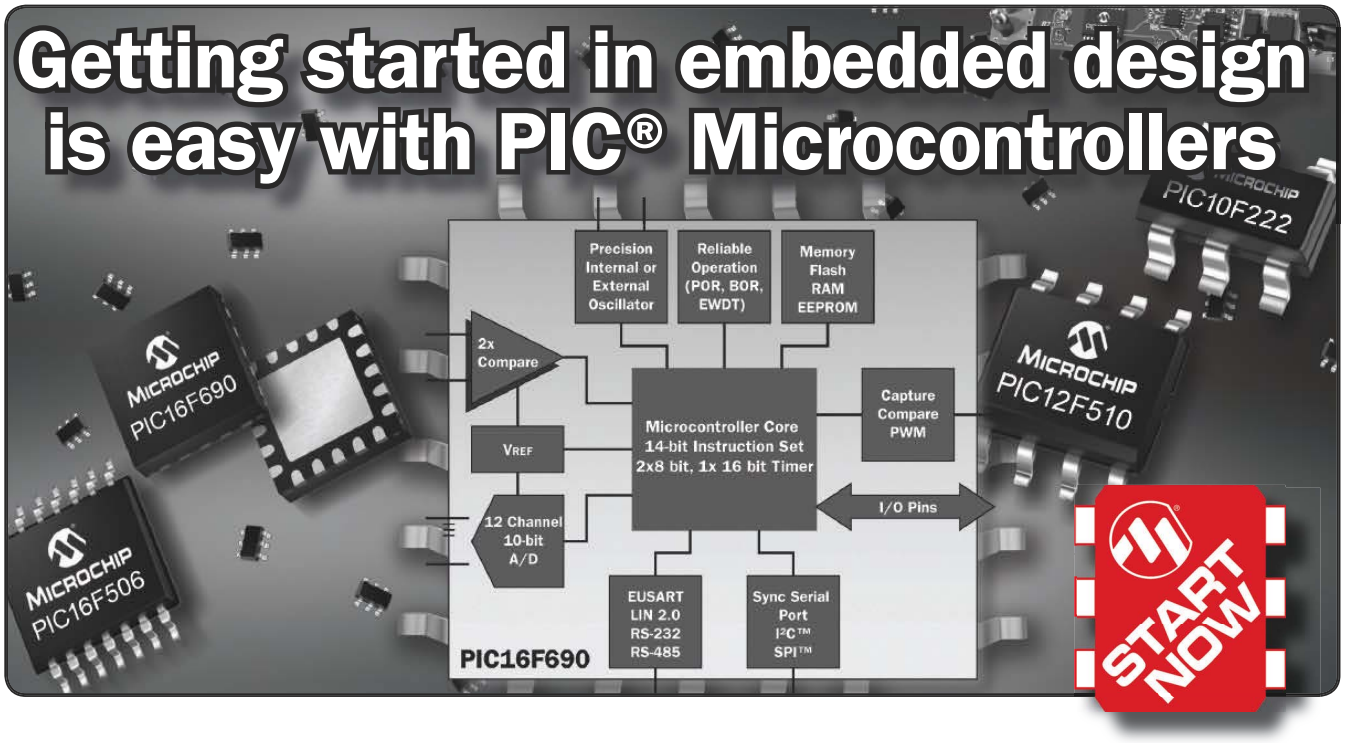

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	PIC12F	12-bit	8	768 to 1536	4 to 8 MHz	8-bit	⊙			
	PIC16F	12-bit	14 to 40	768 to 2048	4 to 8 MHz	8-bit	⊙			
Peripheral-Rich Mid-Range PIC Microcontroller	PIC12F	14-bit	8	1792 to 2048	32 kHz to 8 MHz	10-bit	⊙	⊙	⊙	⊙
	PIC16F	14-bit	14 to 64	1792 to 14336	32 kHz to 8 MHz	10-bit	⊙	⊙	⊙	⊙

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Designers may want to consider custom encoding as a variation of the minimum-encoding style, which adds extra bits or registers to accomplish power, area, or timing goals. It does not have to follow the one-hot- or Gray-encoding style, and designers should not use it unless the project's performance requirements justify its use.

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Moore and Mealey are two FSM styles operating from an output perspective. The output logic of a Moore FSM is only a function of the state registers, whereas the output logic of a Mealey machine is a function of FSM inputs and state registers. It is safer to design a Moore machine. If a design requires a Mealey machine, the designer must thoroughly validate the output logic and the higher level module using the FSM. It is important to watch for any failures resulting from asynchronous behavior of the FSM outputs.

NEXT-STATE LOGIC

Another way to look at FSMs is from a next-state-logic perspective. In simple FSMs, each state is a macro that represents the encoding of the FSM, and each assignment to a next-state variable is a direct assignment to these macros. When a designer directly assigns the next-state variable to a state macro, the logic involved in the next-state calculation comes from conditional statements preceding the assignment and the state's encoding. For code clarity, use simple assignments for next-state variables in an FSM.

However, in some cases, the next state may not use a simple assignment, such as when an FSM requires a complex next-state scheme requiring heavy logic computation. In these cases, the FSM may compute the next state in a separate function or task to simplify or modularize the code. In some cases, a designer may use the function to compute FSM outputs. These extensions indicate FSM complexity, and designers should avoid them whenever possible by decomposing and simplifying the FSM.

The FSM may also compute the next state by using arithmetic or logic operators. The most common arithmetic operation is assigning the next state as the current state incremented by a constant value. This next-state-computation scheme hides complexity. There may be more states than items in the case statement defining the FSM because each next-state calculation may engender a new state that the items lack. This next-state-computation scheme becomes even more complex when it appears in the default item of the case statement.

An FSM may have one or more initial states. As a general rule, an FSM should have an initial state, and the designer should integrate a reset signal into the FSM description to initialize the FSM. An FSM without a standard initial state is susceptible to functional problems and can introduce extra difficulty in analysis, verification, and maintenance.

VALIDATION

Given how FSM features can impact the verification and implementation of a design, it is important to automate the validation methodology so that systematic controls enforce an FSM-design style for a project. The validation tools must automatically detect functional issues in FSMs. The tool should check not only coding styles and syntax, but also potential functional problems, such as deadlock states. Once the tool identifies a bug or problem area, a comprehensive debugging environment needs to perform a root-cause analysis. This debugging environment should support a clear messaging mechanism, RTL-code back annotation, schematic highlighting, an FSM-bubble-diagram viewer, and a waveform viewer. All of these components must tightly integrate to facilitate debugging and the analysis for FSM-related bugs. The tool should present implementation issues in a succinct chart of easy analysis and an FSM-quality audit. This report should link to the debugging environment for easy access and modification of the associated RTL code, as well as FSM exploration.

FSMs are among the biggest sources of bugs and problems in a design. Designers should carefully analyze the metrics to determine the quality of an FSM with regard to its impact on final implementation and verifiability. For a given project, a designer may choose one or multiple FSM styles to fit the requirements of a project. Additionally, for various FSM attributes, such as the number of states and the number of transitions, the designer should implement an upper limit that supports the project requirement and enables easier verifiability of each FSM.

These requirements define an FSM-design methodology that tools should automatically enforce to remove human errors and reduce the design time, building time, and time to market. By thoroughly understanding the types of FSMs and when to use different styles, designers can develop better FSMs. To avoid costly re-spins, it's important to follow the creation guidelines and look for a good FSM-validation approach. EDN

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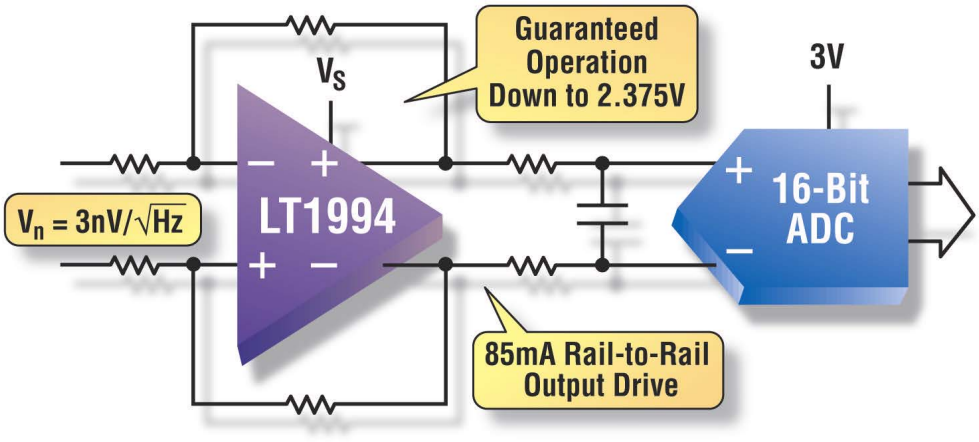

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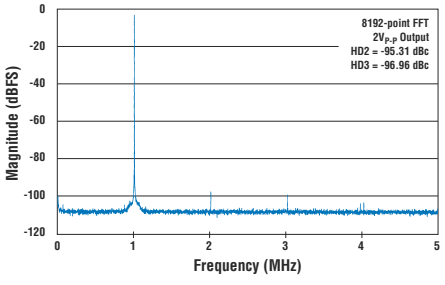

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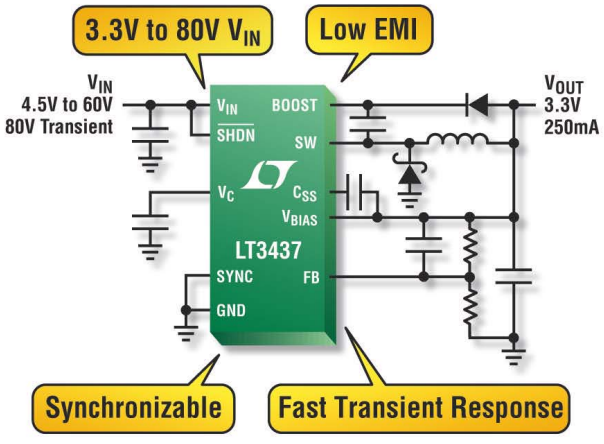

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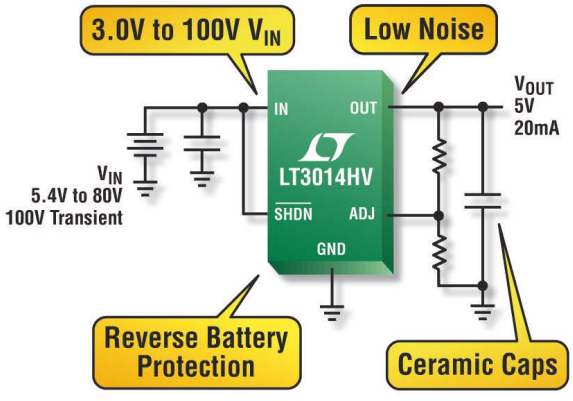

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READERS SOLVE DESIGN PROBLEMS

C oscillator has stable amplitude

Julius Foit, Czech Technical University, Prague, Czech Republic

Many applications call for wide-range-tunable LC oscillators that can deliver a nearly constant-frequency, nearly harmonic-free output even when the circuit's output load changes. From a design viewpoint, eliminating either inductive or capacitive LC circuit taps and transformer couplings within the frequency-determining circuit simplifies fabrication and production, as does the option of grounding one side of the tuned LC circuit. These requirements suggest a circuit that can automatically and efficiently internally adjust loop gain, the basic criterion for oscillation. In addition, the circuit must provide sufficient gain to oscillate with low-impedance LC circuits and regulate the oscillation's amplitude to improve frequency stability and minimize THD (total harmonic distortion).

Designers have exploited many circuit topologies—some highly complex—in their attempts to achieve these design goals, but certain active devices' basic properties can help designers obtain acceptable behavior from a simple oscillator circuit. **Figure 1** shows a basic LC-oscillator arrangement. The amplifier operates as a noninverting voltage-controlled current source. The LC circuit converts the amplifier's output current, I_{OUT}, to voltage, V_{IN}, and applies it as input to the amplifier. **Equation 1** shows the formal condition for oscillation:

$$A_O = \frac{I_{OUT} R_D}{V_{IN}} \geq 1. \qquad (1)$$

In this **equation**, A_O is the overall voltage amplification and R_D is the LC circuit's dynamic resistance at its resonant frequency. In practical circuits, the value of R_D depends on the LC circuit's properties and thus can fall anywhere within a wide range. Also, **Equation 1** assumes an ideal amplifier—that is, one having characteristics that are independent of frequency.

Figure 1 and **Equation 1** yield a simple insight into the basic design problem: If the operation over a wide frequency range demands the use of several LC circuits with widely varying values of R_D, the amplifier's properties must be adjustable over a wide range. You can adjust the amplification to fulfill the gain-limitation condition for the worst-case LC circuit and then rely on device nonlinearities to reduce amplification under overdrive conditions. However, a heavily overdriven amplifier's input- and output-differential resistances can drop to a fraction of their optimum, high-resistance values. Second, large amounts of nonlinear distortion can impair frequency stability. Moreover, these effects depend

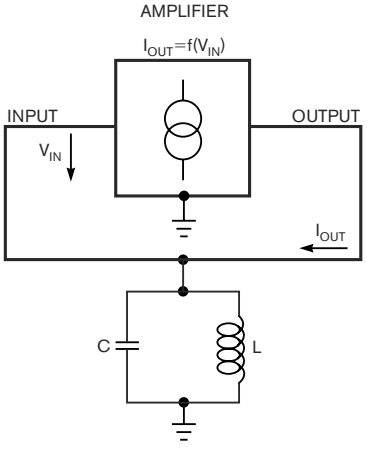

Figure 1 A parallel LC circuit and an amplifying voltage-to-current converter form a basic oscillator.

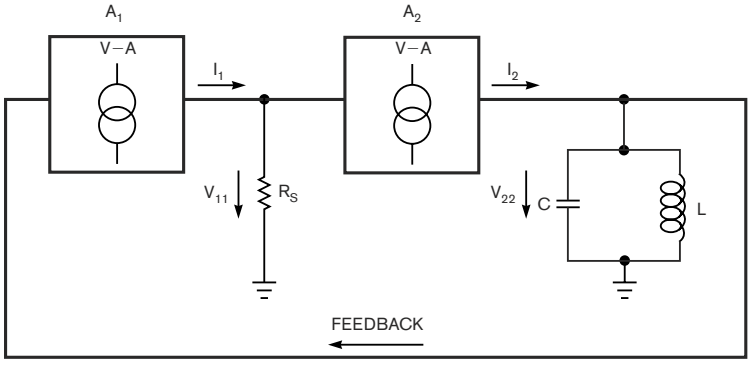

Figure 2 Adding a second voltage-to-current converter isolates the tuned circuit.

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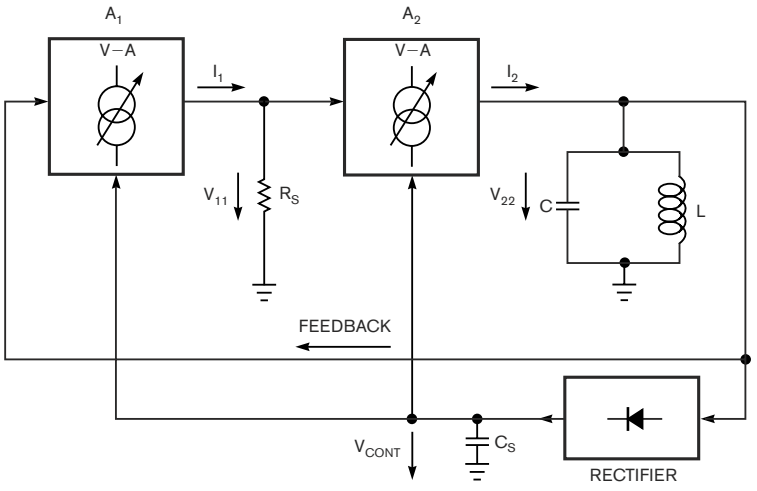

Figure 3 Rectifying a portion of the signal provides a gain-control voltage for the amplifiers.

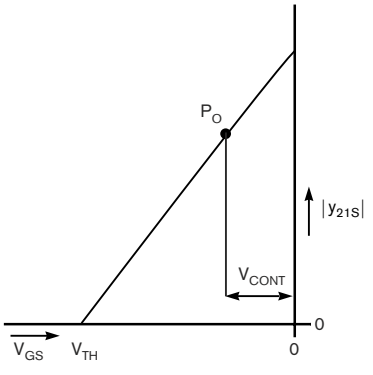

Figure 4 Control characteristics of an idealized JFET exhibit linear variation of forward transconductance versus gate-to-source voltage.

heavily on the amplifier's power-supply voltage, causing frequency stability to deteriorate if the supply voltage varies with load.

Various oscillator circuits use different designs within the amplifier block in **Figure 1**. The popular common-emitter or common-source transistor stage presents two important drawbacks: First, it's an inverting amplifier, and, second, its output does not behave as a good current source, especially when heavily overdriven. Attempts to avoid these problems include transformer coupling or providing impedance-matching taps on the LC circuit, both of which complicate the design and only partially solve the problems.

As **Figure 2** shows, another oscillator topology features two cascaded noninverting amplifiers, A_1 and A_2, as voltage-to-current converters (voltage-controlled current sources). In the circuit, coupling resistor R_S converts amplifier A_1's output current, I_{IN}, to voltage V_{IN}, and drives the second stage, A_2. The tuned circuit's dynamic resistance converts A_2's output current to output voltage, V_{22}, which feeds back to A_1's input to complete the positive-feedback loop. The overall loop amplification, A_{TOTAL}, appears in **Equation 2**:

$$A_{TOTAL} = A_1 \times A_2 = R_S R_D |y_{21S1}| \times |y_{21S2}|. \quad (2)$$

In this **equation**, $R_D = Q\omega L$ is the dynamic resistance of the LC circuit at resonance at the ω frequency, Q is the quality factor of the LC circuit, A_1 and A_2 are the equivalent voltage amplifications of both amplifier stages, and $|y_{21S1}|$ and $|y_{21S2}|$ are the real parts of differential-forward-transfer admittances of both amplifying stages. For self-sustained oscillations, the basic condition $A_{TOTAL} > 1$ in **Equation 1** must apply for all values of the LC circuit's dynamic resistance, R_D. In theory, this condition presents no problem; however, in practice, a situation arises in which the circuit must operate as an LC oscillator with a broad range of tuning inductances and capacitances; a wide range of tuned-circuit quality-factor Q, which the inductor primarily determines; a constant-amplitude output at any combination of conditions A and B; and the best possible frequency stability versus supply voltage and load.

Most LC oscillator circuits cannot simultaneously fulfill all of these requirements. Some oscillator circuits can sequentially fulfill some requirements, but none can fulfill all of them without complicating the circuit beyond reasonable limits. **Figure 3** shows a circuit deriving an external dc control signal from V_{22} to control the voltage-to-current-conversion coefficients—that is, amplification factors—of A_1 and A_2. Applying amplification control to both stages considerably increases the control's effectiveness. In addition to the original positive feedback for starting and sustaining oscillation, you can add an indirect negative-feedback path to the oscillator circuit to limit V_{22}'s amplitude. To meet the original design goals, amplifier blocks A_1 and A_2 should exhibit voltage-controlled input-versus-output characteristics, should possess linear-control amplification characteristics (**Figure 4**), should not invert the signal's phase, and should draw nearly no input current. Also, to emulate a current source, A_2 should present the highest possible differential internal output resistance.

The best active devices for both amplifier stages are the selected N-channel, medium-grade BF245Bs JFETs with a drain current of 5 mA at a gate-to-source voltage of 0V and a drain-to-source voltage of 15V. **Figure 5** shows the final circuit, in which Q_2 operates as a common-drain amplifier, A_2, and Q_1 operates as a common-gate amplifier, A_1.

The gate-source junction of Q_1 rectifies the ac voltage, V_{22}, across the tuned circuit. Coupling capacitor C_4

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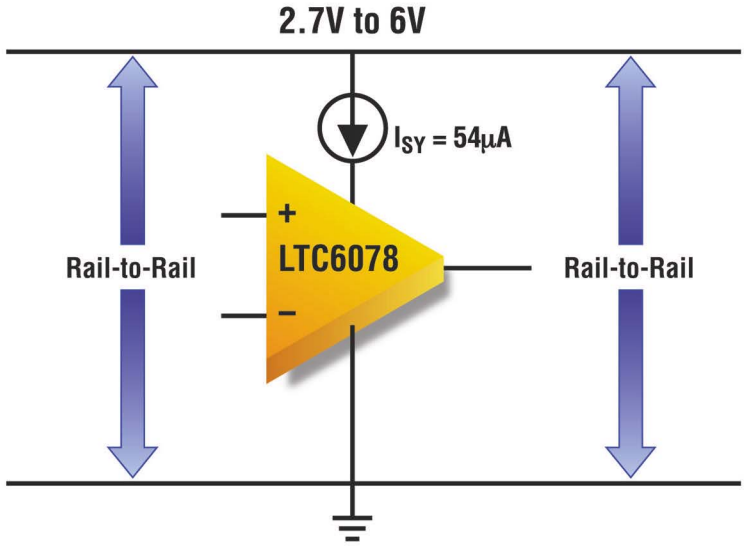

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- Bias Current: 1pA Max.
- Rail-to-Rail In/Out
- CMRR: 95dB Min.
- PSRR: 100dB Min.
- Micropower: 54µA Typ.
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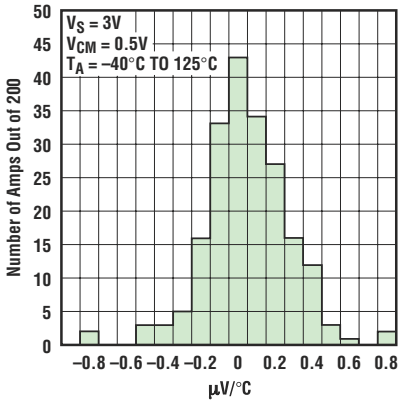
  Quad in SSOP and DFN
- 1k Pricing from $1.49 (Dual)

V_{OS} Drift Distribution



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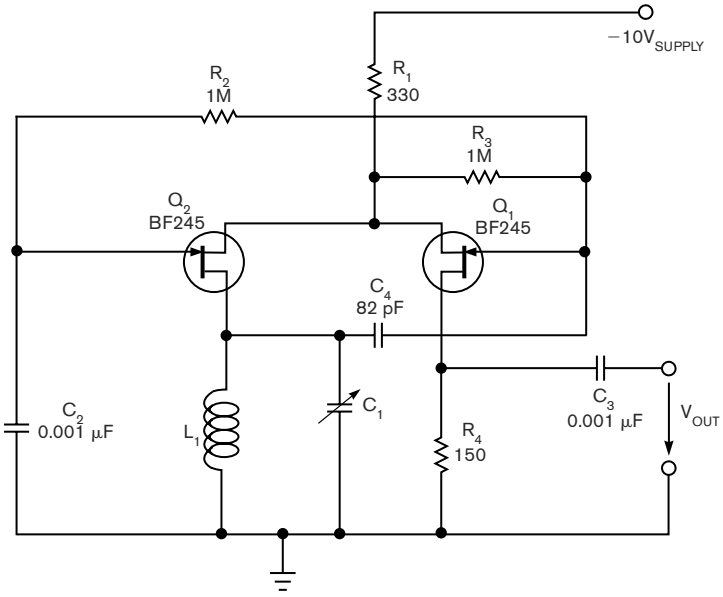


Figure 5 The completed oscillator circuit features a minimal component count.

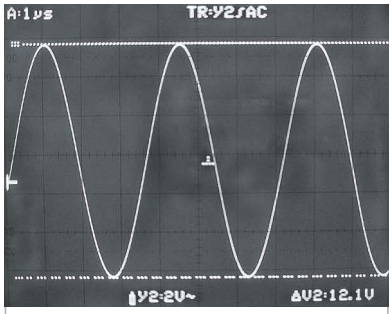
in **Figure 5** doubles as dc-voltage-smoothing capacitor C_S in **Figure 3** because its bottom electrode connects to ground through the low dc resistance of tuning coil L. The dc-control voltage drives the gate of Q_2 through resistor R_2. Capacitor C_2 connects Q_2's gate to ground for ac signals, and Q_2 operates in common-gate connection because Q_1's source drives Q_2's source. To minimize frequency variations due to changing loads, a relatively low-value resistor, R_4, in series with Q_1's drain, isolates the output from the circuit's frequency-determining components. In addition, one lead each of L and C connects to ground.

The waveforms in **Figure 6a** and **6b** show no substantial change in the voltage across the tuned circuit even for widely different values of L and C. The voltage across the tuned circuit remains constant within 3% over a supply-voltage range of 8 to 30V. The same or better amplitude stability holds for the output voltage (**Figure 6c**), even at frequencies as low as 5 kHz and as high as 50 MHz with no adjustment of any passive-component values, except for L and C. Reducing the value of R_4 yields a smaller output voltage, further diminishing the effects of load variations on the operating frequency.

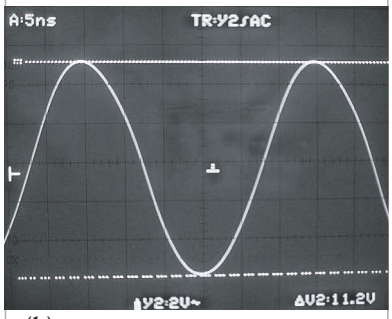
The dc level of the top, flat part of V_{OUT} rests at ground potential, and the waveform goes negative due to the negative power-supply voltage. Because of automatic-gain-control action, the waveshape remains remarkably consistent, regardless of frequency, exhibiting slightly rounded corners, mostly due to stray capacitances, at frequencies higher than 25 MHz. Only the LC circuit's ungrounded end provides a perfect sine wave. Other voltage and current waveforms exhibit cutoff distortion because both transistors operate roughly in Class B mode, shifting toward Class C at increasing power-supply voltages. You can extract a sine wave directly from the LC circuit, but variations in load impedance will influence the operating frequency.

On the other hand, the negative dc feedback controlling the gain of both transistors prevents even relatively large-load-impedance variations across the tuned circuit from greatly affecting the generated amplitude until the LC circuit's Q factor drops very low. At the expense of added complexity and a larger component count, you can include a buffer stage and extract a true sine wave from the LC circuit, but, in the circuit's original application as a radar-marker generator, the constant output amplitude ranked as of greater importance than the waveshape. EDN

(continued on pg 100)



(a)



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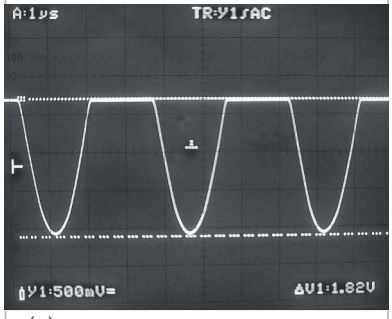

(c)

Figure 6 A clean sine wave (V_{22} in Figure 3) appears across the tuned circuit at 280 kHz for values of 147 µH and 2200 pF for L_1 and C_1, respectively (a). The sine wave with respective values of 56 µH and 60 pF differ (b). The output waveform at 280 kHz, for values of 147 µH for L_1 and 2200 pF for C_1, exhibits a flat top (c).

LINEAR TECHNOLOGY

DESIGN NOTES

Monitor and Protect Automotive Systems with Integrated Current Sensing – Design Note 374

John Munson

Introduction

An automobile is an unforgiving environment for integrated circuits, where under-the-hood operating temperatures run from –40°C to 125°C and large transient excursions on the battery voltage bus are expected. In the past, electronics were part of the well-protected and centralized Engine Control Unit (ECU), but the trend is toward more distributed electronics. Electrically driven accessories and fault-protection monitoring functions are leaving the protective umbrella of the ECU and migrating directly into vehicle subsystems.

For example, many functions formerly driven by the engine—via belt and pulley or hydraulics—are now electrically driven (motorized), such as water pumps, steering mechanisms, brake actuators and various body controls. These functions can become a safety risk if they are not continually monitored for operational readiness and/or have a back-up mode of operation. In either case, real-time monitoring becomes necessary and generally involves accurately measuring the current draw of each subsystem.

Simple Current Monitoring Solutions

The LT®6100 and LTC6101 are high side current-sense amplifiers that have been developed specifically to address the automotive designers' needs. These parts require a minimum number of support components to operate in the harsh automotive battery-bus environment.

Figure 1 shows a basic high side current monitor using the LTC6101. The selection of R_{IN} and R_{OUT} establishes the desired gain of this circuit, powered directly from the battery bus. The current output of the LTC6101 allows it to be located remotely to R_{OUT}. Thus, the amplifier can be placed directly at the shunt, while R_{OUT} is placed near the monitoring electronics without ground drop errors.

This circuit has a fast 1µs response time that makes it ideal for providing MOSFET load switch protection. The switch element may be the high side type connected between the sense resistor and the load, a low side type between the load and ground or an H-bridge. The circuit is programmable to produce up to 1mA of full-scale output current into R_{OUT}, yet draws a mere 250µA supply current when the load is off.

Figure 2 shows the LT6100 used as a combination current sensor and fuse monitor. This part includes on-chip output buffering and was designed to operate with the low supply voltage (≥2.7V), typical of vehicle data acquisition systems, while the sense inputs monitor signals at the higher battery bus potential. The LT6100

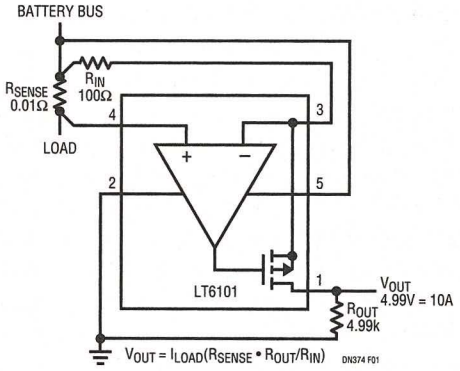

Figure 1. Simple LTC6101 High Side Current Sense Amplifier

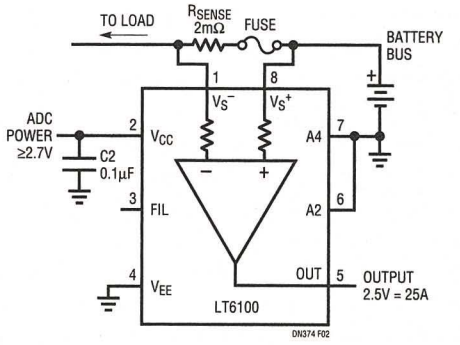

Figure 2. Simple LT6100 High Side Current Sense Amplifier and Fuse Monitor

inputs are tolerant of large input differentials, thus allowing the blown-fuse operating condition (this would be detected by an output full-scale indication). The LT6100 can also be powered down while maintaining high impedance sense inputs, drawing less than 1μA max from the battery bus.

Solving the H-Bridge Problem

Many of the newer electric drive functions, such as steering assist, are bidirectional in nature. These functions are generally driven by H-bridge MOSFET arrays using pulse-width-modulation (PWM) methods to vary the commanded torque. In these systems, there are two main purposes for current monitoring. One is to monitor the current in the load, to track its performance against the desired command (i.e., closed-loop servo law), and another is for fault detection and protection features.

A common monitoring approach in these systems is to amplify the voltage on a "flying" sense resistor, as shown in Figure 3. Unfortunately, several potentially hazardous fault scenarios go undetected, such as a simple short to ground at a motor terminal. Another complication is the noise introduced by the PWM activity. While the PWM noise may be filtered for purposes of the servo law, information useful for protection becomes obscured. The best solution is to simply provide two circuits that individually protect each half-bridge and report the bidirectional load current. In some cases, a smart MOSFET bridge driver may already include sense resistors and offer the protection features needed. In these situations, the best solution is the one that derives the load information with the least additional circuitry.

Figure 4 shows a differential load measurement for an ADC using twin unidirectional sense measurements. Each LTC6101 performs high side sensing that rapidly responds to fault conditions, including load shorts and MOSFET failures. Hardware local to the switch module (not shown in the diagram) can provide the protection logic and furnish a status flag to the control system. The two LTC6101 outputs taken differentially produce a bidirectional load measurement for the control servo. The ground-referenced signals are compatible with most ΔΣ ADCs. The ΔΣ ADC circuit also provides a "free" integration function that removes PWM content from the measurement. This scheme also eliminates the need for analog-to-digital conversions at the rate needed to support switch protection, thus reducing cost and complexity.

Conclusion

The LT6100 and LTC6101 high side current-sense amplifiers simplify designs in the automotive environment. High transient voltage tolerance (105V for the LTC6101HV) and ground-referenced outputs make it possible to improve robustness and substantially reduce the parts-count over traditional solutions.

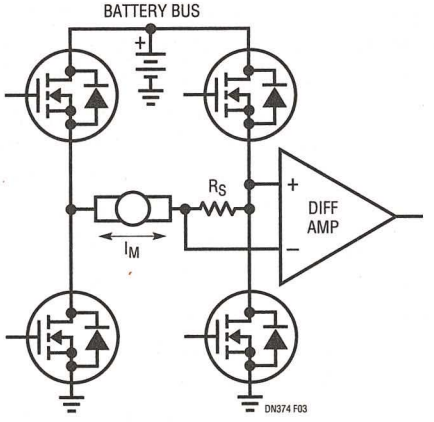

Figure 3. Limited Performance H-Bridge Current Monitor

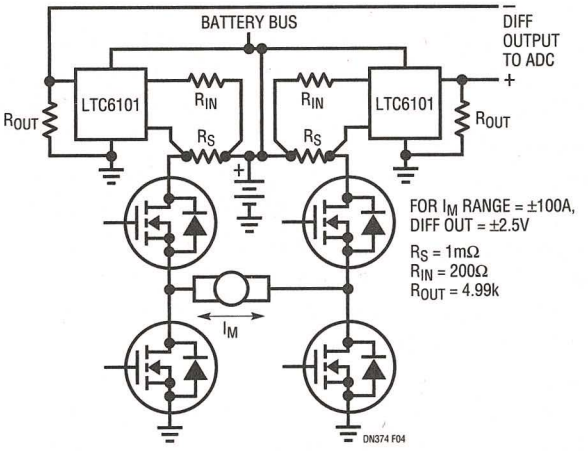

Figure 4. Practical H-Bridge Current Monitor Offers Fault Detection and Bidirectional Load Information

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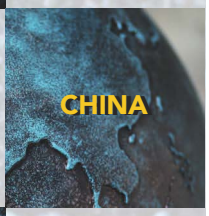

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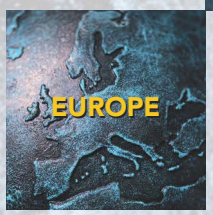

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COMING NOVEMBER 2005

Use a system's real-time clock to "hide" a code sequence

Mihaela Costin, Delmhorst Instruments, Towaco, NJ

Although the concept of a totally accessible system represents an ideal situation for users, designers now must limit access to—and conceal code sequences for—software routines for calibration, diagnostics, memory erasure, system reset, and more. In a system that includes a computer-compatible interface, such as an RS-232, a GPIB, or an infrared-I/O port, the system's software can detect unique input patterns and execute the "secret" code sequences. But if a system lacks a data port, any attempt to implement a secret-access feature in a publicly accessible user interface makes it transparent to the user, even if the feature includes password protection. This Design Idea offers an efficient way to activate a code sequence without making the customer aware that such a feature exists and without requiring any hardware modifications.

If a system includes an RTC (real-time clock), you can define a date and time stamp that invokes the hidden code. The date acts as a password, and, if you choose a date far in the past, a casual user would be unlikely to stumble across it. To implement the routine, you can modify the system software by inserting a date- and time-check routine at the location in which the hidden code executes. Under normal conditions, the program skips the hidden code and executes the routine only if the system's date matches the one that the routine specifies.

For example, the following pseudocode illustrates the use of Aug 12, 1980, as a system "password":

```
Check_date:
  if (Read_RTC(year) ==1980 and
  Read_RTC(month) ==8 and
  Read_RTC(day) ==12)
                run_hidden_sequence();
  Continue_the_Code();
```

After completing the procedure, you must remember to reset the system's clock to the current date and time. Otherwise, the system executes the special code for the remainder of the day until the clock rolls over to the next day. EDN

Shunt regulator eases power-supply-start-up woes

Michael O'Loughlin, Texas Instruments, Nashua, NH

The popular and multiply sourced TL431 three-terminal shunt regulator offers designers considerable versatility in its applications. **Figure 1a** illustrates the TL431's internal circuitry, which comprises a precision voltage reference, an operational amplifier, and a shunt transistor (**Reference 1**). In a typical voltage-regulator application, two external resistors, R_A and R_B, determine the shunt-regulated output voltage at the lower end of load resistor R_S (**Figure 1b**). By way of illustration, the TL431 and a few external active and passive components can serve as a low-power auxiliary power supply for an SMPS (switched-mode-power-supply) PWM (pulse-width-modulated) controller. In some power-supply designs, an auxiliary winding on the step-down transformer supplies power to the PWM controller. Under light output loads, the auxiliary winding may supply inadequate power to the PWM controller. For example, the converter circuit in **Figure 2** derives power for PWM controller IC_1 through an auxiliary bias winding, W_{AUX}, which is part of transformer T_1. Resistor R_T and capacitor C_{HOLD} form a trickle-charge circuit that supplies start-up power to IC_1. To conserve energy, resistor R_T supplies just enough current to trickle-charge C_{HOLD} to voltage V_{AUX}. Once the circuit starts, it

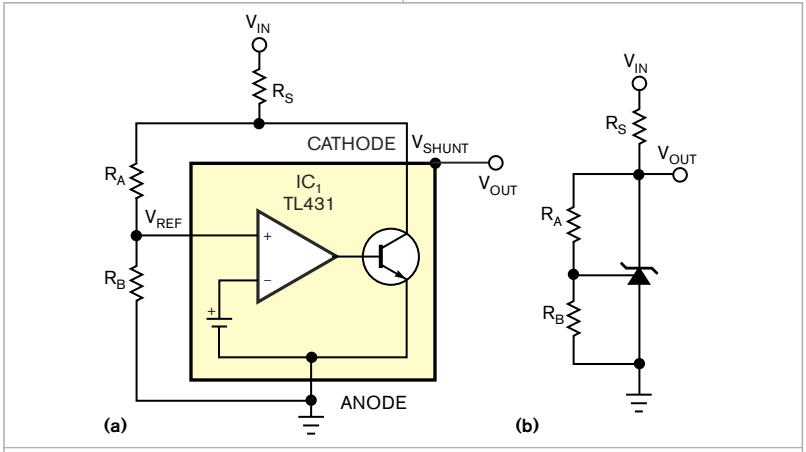

Figure 1 An uncomplicated block diagram (a) conceals the TL431's internal complexity, but you need only three external resistors to use the TL431 in a basic shunt-regulator circuit (b).

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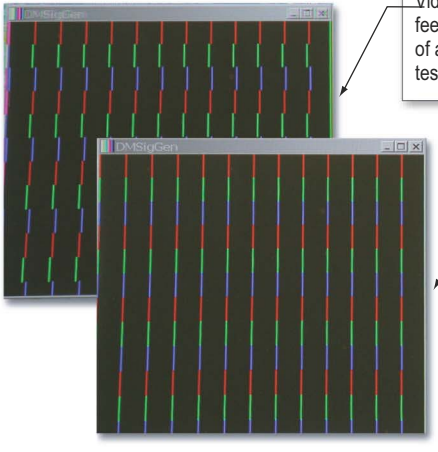

Video transmitted over 1000 feet of CAT-5. Note the lack of alignment on the RGB test pattern.

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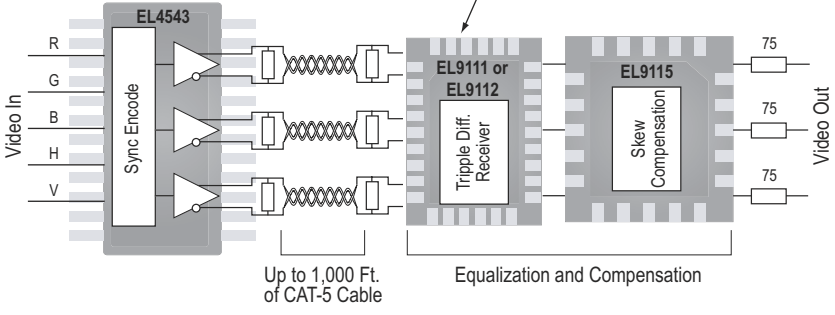

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operates as you would expect and delivers output power to the load, and the auxiliary winding and its components power the PWM controller.

However, removing the output load reduces the energy supplied to the auxiliary bias winding, depleting the charge on C_{HOLD} and causing IC_1 to turn off, which in turn upsets output-voltage regulation and causes the power supply to operate erratically. A low-power bias-supply circuit supplies light-load start-up power and then switches off to conserve power whenever the auxiliary winding can supply enough energy to PWM controller IC_1 (**Figure 3**). In this circuit, a series-pass regulator turns on under light-load conditions and turns off when the bias winding can supply the energy to the PWM controller, thus conserving energy under load and improving converter efficiency.

Resistors R_A through R_D, shunt regulator IC_1, diode D_1, and transistor Q_1 form the low-load series-pass-regulated bias supply. You select these components to produce a voltage at Q_1's emitter that falls between IC_1's turn-off voltage and the nominal voltage produced by rectifying the auxiliary bias winding's output, V_{AUX_NOM}. In effect, the voltage at IC_1's V_{CC} pin follows in wired-OR fashion whichever is higher: V_{AUX_NOM} or the voltage at transistor Q_1's emitter. When the auxiliary bias winding and its components deliver sufficient power, Q_1's emitter sees a reverse bias, and Q_1 shuts off to conserve energy. Conversely, Q_1 supplies power when V_{AUX} decreases below V_{AUX_NOM} due to a light output load. Note that the circuit still must include trickle-charge resistor R_T because most PWM controllers incorporate undervoltage lockout, the ability to start at a higher than nominal supply voltage.

To design the series-pass regulator, select resistor R_C to supply sufficient operating current to IC_2, and select resistor R_D to maintain Q_1's collector voltage and current within its safe operating area. Select resistors R_A and R_B to set the series regulator's output voltage above IC_1's start-up voltage and below the nominal voltage supplied by the auxiliary winding's rectified output. Choose bypass capacitor C_A to minimize ripple voltage across IC_2.

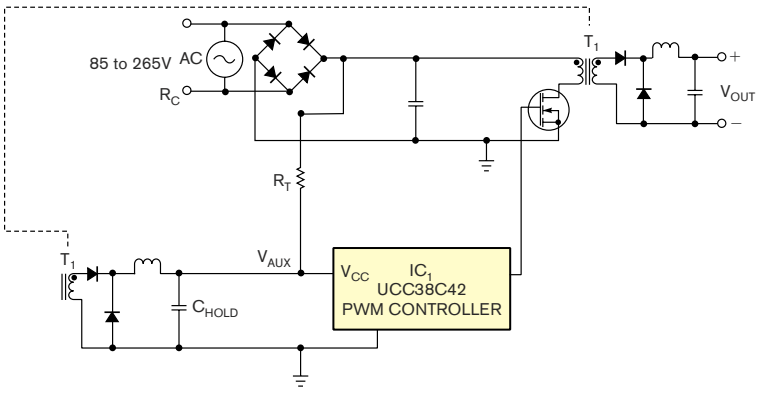

Figure 2 An auxiliary winding supplies power to the supply's PWM controller.

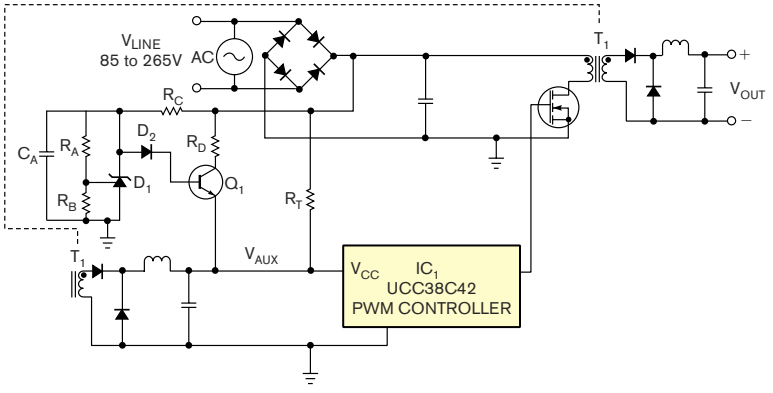

Figure 3 In this improved design, pulse-width-controller IC_1 derives its power from R_T for start-up, auxiliary winding W_{AUX} for normal operation, and shunt-regulator circuit IC_2 and Q_1 for low-load operation.

You can use the following **equation** to adjust the voltage divider formed by resistors R_A and R_B:

$$\frac{V_{REF}}{R_B} = \frac{V_{AUX\_NOM} - V_{DI} - V_{BE(Q_1)} - V_{REF} - 1V}{R_A}.$$

The voltage at Q_1's emitter must fall below the nominal auxiliary voltage, which the auxiliary bias winding supplies. V_{REF} represents shunt regulator IC_2's internal nominal reference voltage of 2.495V, and V_{D1} and $V_{BE(Q1)}$ represent D_1's voltage drop and Q_1's forward base-emitter voltage, respectively. EDN

REFERENCE

1 O'Loughlin, Michael, "Shunt regulator serves as inexpensive op amp in power supplies," *EDN*, Sept 15, 2005, pg 96, www.edn.com/article/CA6255051.

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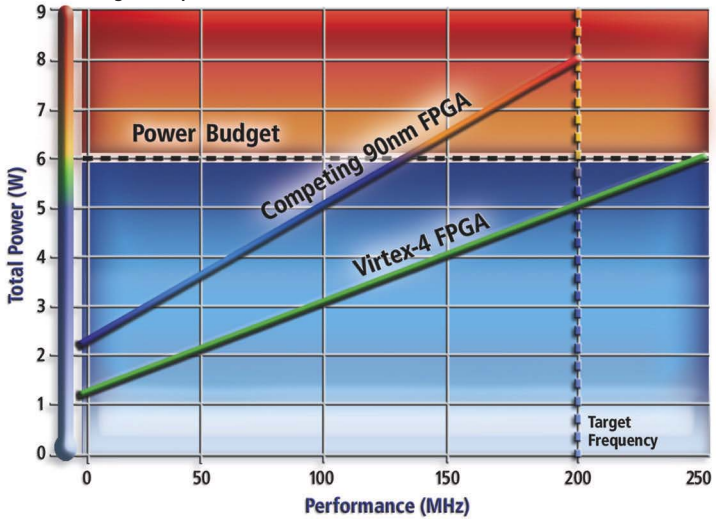

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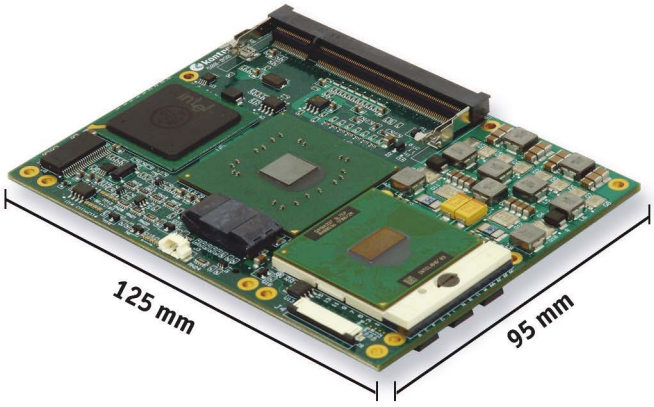

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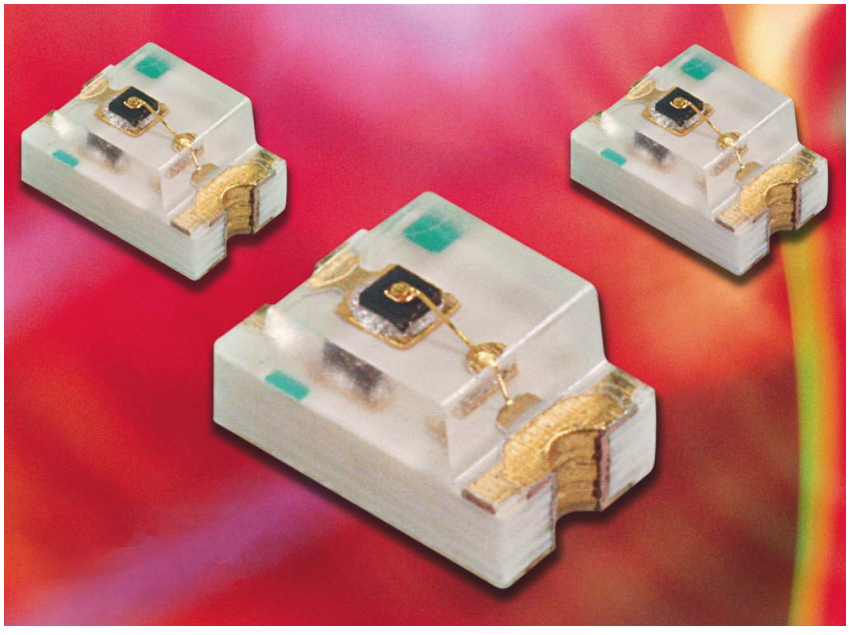

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Optek Technology, www.optekinc.com

Backlights use one LED for backlight color and monochrome LCDs

These white, single-LED backlights provide light for color and monochrome LCDs. The units can have a diagonal measurement of 0.25 to 4.7 in. The devices incorporate the vendor's MicroLens pixel-based light-extraction technology. Measuring 0.6 mm thick, the backlights cost $1.20 for a 1.5-in.-diagonal unit for cell-phone displays and $1.75 for backlights in a monochrome digital-thermostat display.

Global Lighting Technologies, www.glthome.com

LED has 50-mA drive current

The white-emission LTWE670DS color LED features heat-management technology that allows it to accommodate currents as high as 50 mA. The LED generates 3000 mcd and has a 120° viewing angle. The lead-free, ROHS (reduction-of-hazardous-substances)-compliant device comes in various light intensity/brightness and hue/chromaticity coordinates.

LiteOn Inc, www.us.liteon.com

3W power-LED module features 90-lumen brightness

Based on Cree Xlamp technology, the 3W LK3 series LED module comes in a metal-core pc-board base. The device has a 100° viewing angle with full-spectrum wavelengths from 465 to 635 nm and in white to 8000K. Additional peripherals include a 700-mA maximum I_f rating and a 90-lumen brightness. The LK3 module costs $6.

BivarOpto, www.bivar.com

Surface-mount RGB LED features water-clear lens for diode protection

With a low profile, the SML5050-RBG1K-TR surface-mount, full-spectrum RGB LED measures 5.5×5.5 mm. Emitting high-intensity light in a 120° viewing angle, the LED features 150 to 500 mcd luminous intensities at a 20-mA current, depending on the color. A water-clear lens protects the diode array. The SML-5050RBG1K-TR SMT LED costs $2.15.

LEDtronics, www.ledtronics.com

8.4-in. TFT LCD suits industrial use

Measuring 8.4 in., this amorphous-silicon, TFT (thin-film-transistor), VGA-resolution LCD features a 400-cd/m^2 luminance and a 72% color gamut, equivalent to a CRT. The device has a viewing angle of 170° and a −10 to +70°C operating-temperature range.

NEC Electronics America Inc, www.am.necel.com

FPGA-based processor PMC includes memory and high-speed data I/O

Targeting SDR (software-defined-radio) and DSP applications, the ICS-1580 baseband-processing engine employs a user-programmable Xilinx Virtex II Pro FPGA surrounded with memory and high-speed data I/O. The device also includes four banks of SDRAM, four banks of high-speed QDRII SRAM, and two 128-Mbit flash-memory units. It provides a 64/66 PCI interface, as well as high-speed serial-switched-fabric capabilities, enabling an aggregate bandwidth of 25 Gbps.

Radstone Embedded Computing, www.radstone.com

Video-control-processor IP suits hard-disk formats

The programmable SVEN (scalable-video-engine) platform complies with video-decoder standards, including H.264, VC-1, and MPEG-2 for resolutions of 1080i and 720p. The product features a video-processing engine, a picture-memory controller, IP (intellectual property) for process-entropy-decoding tasks, and a binarization extension. The video-control processor uses multiple-instruction, multiple-data control to provide parallel-processing slots; each slot has its own data memory. The processor uses a three-stage instruction pipeline, permitting two neighboring slots to work in parallel to allow conditional executions within one cycle.

On Demand Microelectronics, www.ondemand.co.at

Processor targets ZigBee-network applications

Targeting processor-intensive ZigBee applications that benefit from a dedicated microcontroller, the EM260 network processor features an EmberZNet 2.0 networking stack. The EmberZNet 2.0 includes a transport layer for wireless communications and supports application profiles for home controls and user-defined network applications. A development kit with distributed network-debugging and visualization tools allows users to upload firmware and collect debugging information simultaneously across multiple devices. The EM260 costs $3.50.

Ember Corp, www.ember.com

Video-optimized IP cores target handheld semiconductor design

Adding to the Mali line of smart pixel-processing cores, the Mali video series comprises the Mali 110V, Mali 55V, and Mali GP-V geometric-processing core. These pixel-processing cores function with the ARM core to accelerate video encoding and decoding to 30 frames/sec, as well as handle motion estimation, motion compensation, video scaling, image differencing, and color-space-conversion tasks. Suited for handheld-semiconductor design, the cores include an out-of-the-box software stack that is preverified to support OpenGL ES and Microsoft Direct3D Mobile, along with a performance-analysis tool.

Falanx Microsystems, www.falanx.com

Compiler-development system supports embedded-C extensions

TR 18037 programming languages—C extensions to support embedded processors—specify fixed-point arithmetic, named-address spaces, named-register storage classes, and basic I/O-hardware-addressing support in the C programming language. This embedded-C-language package features front-end support for embedded-C-language extensions, runtime libraries, and intrinsic function libraries for creating embedded-C compilers. Available packages include the CoSy base, DSP-C, Embedded C, C++, advanced optimizations, the CoSy Express generator, ARM CG, Pentium CG, and Sparc CG. Perpetual licenses cost $250,000.

ACE Associated Compiler Experts, www.ace.nl

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Airport gives advanced baggage-handling system the boot

Ongoing problems with the advanced, automated baggage-handling system delayed the opening of the Denver International Airport for 16 months until February 1995. Now-defunct BAE Automated Systems designed the system using the Wonderware InTouch human-machine interface from Invensys Systems Inc. The system's cost zoomed from an estimated total of $185 million to more than $300 million, due to extra engineering and debugging costs, interest, and penalties.

With 26 miles of track, the system was supposed to shunt bags in small, gray carts from source to destination, tracking and steering the carts onto conveyor tracks. A central computer would track carts in real time and would control per-cart steering. But tracking the carts and dealing with inevitable spills, pileups, breakdowns, and other deviations from ideal overwhelmed the system. After years of trying to fix it or work around it, airport officials have shut down the system. They are dismantling its parts and selling them off for scrap. They plan to replace the system with a more manual one employing handheld bar-code readers and lots of people. You can get more details at http://ntl.bts.gov/DOCS/rc9535br.html.—by Bill Schweber

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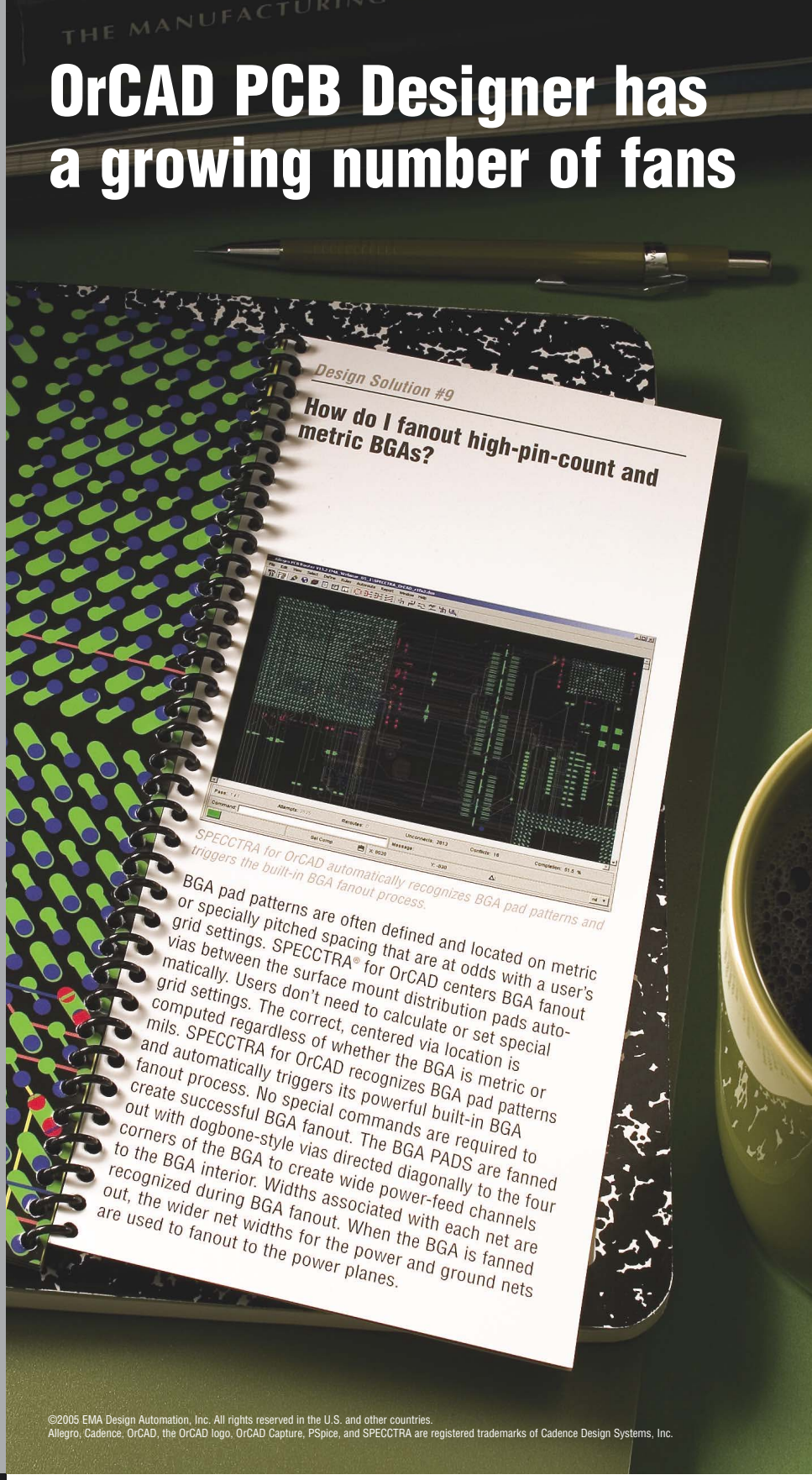

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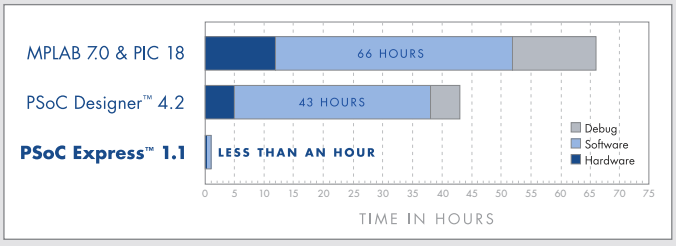

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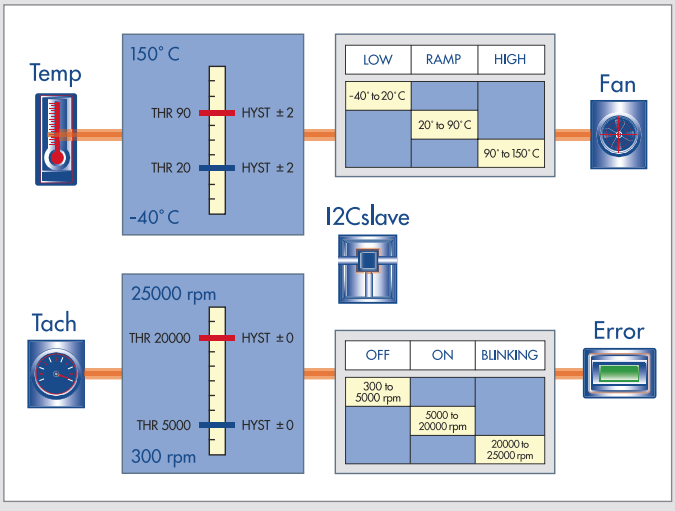

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